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? show files;ds
File 347:JAPIO Nov 1976-2005/Nov(Updated 060302)
         (c) 2006 JPO & JAPIO
File 350:Derwent WPIX 1963-2006/UD,UM &UP=200618
         (c) 2006  Thomson Derwent

Set     Items   Description
S1      12431   (DUMMY OR FAKE OR FALSE OR GARBAGE OR NONSENSE OR JUNK OR -
             RUBBISH OR BOGUS OR PHONY OR MOCK OR MISLEADING OR ERRONEOUS -
             OR AMBIGUOUS OR USELESS)(2W)(INSTRUCTION? ? OR OPERATION? ? OR
              COMMAND? ? OR CODE? ? OR ACTION? ? OR TASK? ?)
S2         83   (DUMMY OR FAKE OR FALSE OR GARBAGE OR NONSENSE OR JUNK OR -
             RUBBISH OR BOGUS OR PHONY OR MOCK OR MISLEADING OR ERRONEOUS -
             OR AMBIGUOUS OR USELESS)(2W)(JOB? ? OR TRANSACTION? ?)
S3       1982   S1:S2(10N)(INTRODUC? OR INPUT???? OR ADD??? OR INSERT??? OR
              ENTER??? OR GENERAT??? OR CREAT??? OR MIX??? OR INTERLEAV???
             OR COMBIN? OR MERG??? OR SLOT???? OR INCORPORAT? OR PRODUC????
              OR INTERSPERS? OR INTERMINGL???)
S4        184   S1:S2(10N)(INTEGRAT? OR MIX??? OR INTERMIX??? OR SPRINKL??-
             ?)
S5     128785   (SUCCEEDING OR SUCCESSIVE OR CONSECUTIV? OR ENSUING OR TWO
             OR 2 OR SECOND???)(5W)(INSTRUCTION? ? OR OPERATION? ? OR COMM-
             AND? ? OR CODE? ? OR ACTION? ? OR TASK? ?)
S6     142899   (THREE OR THIRD OR 3 OR FOUR OR FOURTH OR 4 OR FIVE OR FIF-
             TH OR 5)(5W)(INSTRUCTION? ? OR OPERATION? ? OR COMMAND? ? OR -
             CODE? ? OR ACTION? ? OR TASK? ?)
S7    5618763   TIME? ? OR TIMING OR INTERVAL? ? OR PERIOD? ? OR SECOND? ?
             OR MINUTE? ? OR HOUR? ?
S8          0   PHONEY(2W)(INSTRUCTION? ? OR OPERATION? ? OR COMMAND? ? OR
             CODE? ? OR ACTION? ? OR TASK? ? OR JOB? ? OR TRANSACTION? ?)
S9        111   S3:S4 AND S5:S6 AND S7
S10         1   S9 AND AC=US/PR AND AY=(1963:1999)/PR
S11         5   S9 AND AC=US AND AY=1963:1999
S12         5   S9 AND AC=US AND AY=(1963:1999)/PR
S13       100   S9 AND PY=1963:1999
S14     63422   (SUCCEEDING OR SUCCESSIVE OR CONSECUTIV? OR ENSUING OR TWO
             OR SECOND???)(5W)(INSTRUCTION? ? OR OPERATION? ? OR COMMAND? ?
              OR CODE? ? OR ACTION? ? OR TASK? ?)
S15     14329   (THREE OR THIRD OR FOUR OR FOURTH OR FIVE OR FIFTH)(5W)(IN-
             STRUCTION? ? OR OPERATION? ? OR COMMAND? ? OR CODE? ? OR ACTI-
             ON? ? OR TASK? ?)
S16        36   S13 AND S14:S15
S17        36   IDPAT (sorted in duplicate/non-duplicate order)
S18       489   INVALID(2W)(INSTRUCTION? ? OR OPERATION? ? OR COMMAND? ? OR
              CODE? ? OR ACTION? ? OR TASK? ? OR JOB? ? OR TRANSACTION? ?)
S19        16   S18 AND S14:S15 AND S7
S20       103   S18(10N)(INTRODUC? OR INPUT???? OR ADD??? OR INSERT??? OR -
             ENTER??? OR GENERAT??? OR CREAT??? OR MIX??? OR INTERLEAV??? -
             OR COMBIN? OR MERG??? OR SLOT???? OR INCORPORAT? OR PRODUC????
              OR INTERSPERS? OR INTERMINGL???)
S21         1   S18(10N)(INTEGRAT? OR MIX??? OR INTERMIX??? OR SPRINKL???)
S22         5   S19 AND S20:S21
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17/5/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012901570
WPI Acc No: 2000-073406/ **200007**
XRPX Acc No: N00-057441
Anti- false **bar** code **and** producing **and distinguishing method thereof**
Patent Assignee: HENGMAO COMMERCE & TRADE CO LTD BEIJING (HENG-N)
Inventor: LIU B; LU D; WANG Y
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
CN 1204099	A	19990106	CN 97111878	A	19970628	200007	B

Priority Applications (No Type Date): CN 97111878 A 19970628
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
CN 1204099	A		1	G06K-019/06	

Abstract (Basic): CN 1204099 A
NOVELTY - The anti-false bar code consists of three portions: first portion is commodity classification code, formed from 6-8 places, **second** portion is random commodity unique **code** , formed from 9-12 places, and **third** portion is check **code** , formed from 1 place.
USE - For use as a barcode system.
ADVANTAGES - The system can know the characteristics of every commodity from the invented bar code, can distinguish truth from falsehood and can reflect the characteristic informations of every commodity, such as place of production, date of production, date of sale and storage life, etc..
Dwg.0
Title Terms: ANTI; FALSE; BAR; CODE; PRODUCE; DISTINGUISH; METHOD
Derwent Class: T04
International Patent Class (Main): G06K-019/06
International Patent Class (Additional): G06K-007/00
File Segment: EPI

17/5/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011212895 **Image available**
WPI Acc No: 1997-190820/ **199717**
XRPX Acc No: N97-157815
IR ray type remote controller for door of motor vehicle - has adder **which** combines **modulated** dummy code **and transmitting code and outputs** combined **code to transmitter**
Patent Assignee: OKI ELECTRIC IND CO LTD (OKID); OKI SYSTEK TOKAI KK (OKID)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 9051593	A	19970218	JP 95202060	A	19950808	199717	B

Priority Applications (No Type Date): JP 95202060 A 19950808
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 9051593	A		6	H04Q-009/00	

Abstract (Basic): JP 9051593 A
The remote controller has a **dummy code generator** (11) which **generates** a **dummy code** based on a control signal output from a control unit (10). A first modulator (13) modulates the **generated**

dummy code using a carrier frequency **generated** by a carrier **generator** (12).

A **second** modulator (15) modulates the transmitting **code** generated by a transmitting code generator (32) using the carrier frequency different from the carrier frequency used for modulating **dummy code** . An **adder** (16) **combines** the output of the two modulators and outputs the combined result to a transmitter (35) which transmits the combined codes using IR rays.

ADVANTAGE - Avoids copying of transmitting code by modulating at frequencies different from modulation frequency of dummy code.

Dwg.1/3

Title Terms: INFRARED; RAY; TYPE; REMOTE; CONTROL; DOOR; MOTOR; VEHICLE; ADDER; COMBINATION; MODULATE; DUMMY; CODE; TRANSMIT; CODE; OUTPUT; COMBINATION; CODE; TRANSMIT

Derwent Class: W05; X22

International Patent Class (Main): H04Q-009/00

International Patent Class (Additional): H04K-001/00; H04Q-009/14

File Segment: EPI

17/5/3 (Item 3 from file: 350)

011208115 **Image available**

WPI Acc No: 1997-186040/ **199717**

XRPX Acc No: N97-153552

Encoding device and for processing enciphering/dividing variable length code (VLC) - uses two barrel shifters which generate newly coupled variable length codeword data and segment of constant length to be added to pseudo code length of currently input codeword

Patent Assignee: DAEWOO ELECTRONICS CO LTD (DAEW-N)

Inventor: KWANG D; KANG D S; KANG D

Number of Countries: 004 Number of Patents: 007

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 9046237	A	19970214	JP 95334072	A	19951129	199717	B
KR 97009422	A	19970224	KR 9522590	A	19950727	199812	
US 5754128	A	19980519	US 95560696	A	19951120	199827	
CN 1141538	A	19970129	CN 95117558	A	19951129	200051	
KR 180164	B1	19990501	KR 9522590	A	19950727	200051	
JP 3389391	B2	20030324	JP 95334072	A	19951129	200323	
CN 1108014	C	20030507	CN 95117558	A	19951129	200540	

Priority Applications (No Type Date): KR 9522590 A 19950727

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 9046237	A		9	H03M-007/42	
KR 97009422	A			H04N-007/66	
US 5754128	A			H03M-007/40	
CN 1141538	A			H03M-007/40	
KR 180164	B1			H04N-007/66	
JP 3389391	B2		9	H03M-007/42	Previous Publ. patent JP 9046237
CN 1108014	C			H03M-007/40	

Abstract (Basic): JP 9046237 A

The encoding device has six registers (10,28,30,34,38,42). The source code is stored in the first register. Each source code is mapped to the variable length code. A look-up table (20) generates the corresponding code length. The **second** register generates and stores a variable length codeword. The **third** register generates the stored **code** length in response to an enable signal. A byte alignment unit (200) **generates** a **dummy code** length in response to a byte alignment signal. The dummy code length specifies the number of bits between the starting position of the code and the last bit of the final

segment.
The variable length codeword coupled with the dummy codeword is coupled in response to first control signal, which shows code length or **dummy code** length of the currently **input** variable length codeword. A first barrel shifter (32) generates the variable length codeword which coupled a fresh the currently input variable codeword of the dummy codeword. A **second** barrel shifter (40) generates a data segment of constant length. An adder (36) computes the sum of the code length or the pseudo code length of the currently input variable length codeword. The fifth register generates the output enable signal showing the effectiveness of a data segment. The sixth register generates and stores a data segment of constant length.
ADVANTAGE - Divides variable codeword effectively.
Dwg.1/5

Title Terms: ENCODE; DEVICE; PROCESS; ENCIPHER; DIVIDE; VARIABLE; LENGTH; CODE; TWO; BARREL; SHIFT; GENERATE; NEW; COUPLE; VARIABLE; LENGTH; CODE; DATA; SEGMENT; CONSTANT; LENGTH; ADD; PSEUDO; CODE; LENGTH; CURRENT; INPUT; CODE
Derwent Class: T01; U21
International Patent Class (Main): H03M-007/40; H03M-007/42; H04N-007/66
International Patent Class (Additional): G06F-005/00
File Segment: EPI

17/5/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009829903 **Image available**
WPI Acc No: 1994-109759/ **199413**
XRPX Acc No: N94-085818
Data processor - has two instruction **registers connected in cascade and** two instruction **decoders, decode result generating circuit, execution control unit, and instruction execution unit**
Patent Assignee: HITACHI LTD (HITA)
Inventor: HANAWA M; NARITA S; NISHII O; UCHIYAMA K
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5301285	A	19940405	US 90496448	A	19900320	199413	B
			US 92940762	A	19920904		
KR 163179	B1	19990115	KR 904306	A	19900330	200036	

Priority Applications (No Type Date): JP 8978221 A 19890331
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5301285	A		11	G06F-009/30	Cont of application US 90496448
KR 163179	B1			G06F-009/34	

Abstract (Basic): US 5301285 A
The data processor includes two registers storing a respective halves of a word of one instruction. A first decoder decodes the first half word and at the same **time** detecting whether there exists an addressing extension portion between the first half word and the **second** half word. A **second** decoder decodes the **second** half word. A decode result generating circuit is provided, to which a detection signal of the first decoder indicates whether the addressing extension portion exists. A decode result of the first decoder and a decode result of the **second** decoder are supplied to the decode result generating circuit.
An extension portion register is provided to store the addressing extension portion. When the first decoder detects the addressing extension portion, the decode result generating circuit invalidates the decode result of the **second** decoder. On the other hand, in the case where there exists no addressing extension portion, the decode result generating circuit judges, on the basis of the detection signal, that

the decode result of the **second** decoder is valid.

ADVANTAGE - Can carry out decoding or operation of simple instruction, with no **erroneous operation produced** in decoding or operation of complicated instruction.

Dwg.1/4

Title Terms: DATA; PROCESSOR; TWO; INSTRUCTION; REGISTER; CONNECT; CASCADE; TWO; INSTRUCTION; DECODE; DECODE; RESULT; GENERATE; CIRCUIT; EXECUTE; CONTROL; UNIT; INSTRUCTION; EXECUTE; UNIT

Derwent Class: T01

International Patent Class (Main): G06F-009/30; G06F-009/34

International Patent Class (Additional): G06F-009/34

File Segment: EPI

17/5/8 (Item 8 from file: 350)

008474658 **Image available**

WPI Acc No: 1990-361658/ **199048**

XRPX Acc No: N90-275941

Information code applying method for video tape - encoding information in synchronisation pulses without affecting synchronisation

Patent Assignee: GSE INC (GSEG-N)

Inventor: ROGGENDORF P

Number of Countries: 010 Number of Patents: 008

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9013892	A	19901115				199048	B
AU 9056639	A	19901129				199109	
EP 428659	A	19910529	EP 90907730	A	19900510	199122	
US 5018027	A	19910521	US 89349690	A	19890510	199123	
EP 428659	A4	19920624	EP 90907730	A	19900000	199522	
EP 428659	B1	19951206	EP 90907730	A	19900510	199602	
			WO 90US2625	A	19900510		
DE 69024028	E	19960118	DE 624028	A	19900510	199608	
			EP 90907730	A	19900510		
			WO 90US2625	A	19900510		
CA 2033979	C	19960102	CA 2033979	A	19900510	199613	

Priority Applications (No Type Date): US 89349690 A 19890510

Cited Patents: US 4466029; US 4703311; 2.Jnl.Ref; DE 3149293; US 3681524

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9013892	A				
Designated States (National): AU CA JP					
Designated States (Regional): AT DE FR GB IT NL					
EP 428659	A				
Designated States (Regional): AT DE FR GB IT NL					
EP 428659	B1	E	15	G11B-005/09	Based on patent WO 9013892
Designated States (Regional): AT DE FR GB IT NL					
DE 69024028	E			G11B-005/09	Based on patent EP 428659
					Based on patent WO 9013892
CA 2033979	C			G11B-005/09	

Abstract (Basic): WO 9013892 A

The editing device for 1/2 inch video tapes applies pulse width modulation to prerecorded synchronising pulses in predetermined **intervals** . Each **interval** begins with an eleven bit hear (44) compatible with the VASS system. **Time** codes (58) to identify the recording session and elapsed **time** is added.

A check code (60) completes the modulation for 50Hz systems, e.g. PAL and SECAM, and for 60Hz systems a ten-bit **dummy code** (62) is **added** to complete the **interval** . The leading edge of the synchronising pulse is not affected.

USE/ADVANTAGE - Identifies location on tape within 2 **seconds** and produces compatibility with RAPID, VASS, PAL and SECAM systems. (36pp Dwg.No.3/6)

Title Terms: INFORMATION; CODE; APPLY; METHOD; VIDEO; TAPE; ENCODE; INFORMATION; SYNCHRONISATION; PULSE; AFFECT; SYNCHRONISATION

Derwent Class: T03; W04

International Patent Class (Main): G11B-005/09

International Patent Class (Additional): G11B-005/86; G11B-027/02

File Segment: EPI

17/5/9 (Item 9 from file: 350)

DIALOG(R)File 350:Derwent WPIX

007720182 **Image available**

WPI Acc No: 1988-354114/ **198849**

XRPX Acc No: N88-268416

Error checking method for serial transfer form information signal - using cyclic redundancy check of information signals, dummy codes and attribute flags

Patent Assignee: FUJITSU LTD (FUIT)

Inventor: ENDO K; MIKUNI T; MIYAZAWA K; NISHIMURA K; OKAMOTO K

Number of Countries: 015 Number of Patents: 009

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 8809590	A	19881201				198849	B
AU 8817969	A	19881221				198916	
EP 315699	A	19890517	EP 88904640	A	19880526	198920	
ES 2009048	A	19890816	ES 882960	A	19880929	198950	
JP 2501614	W	19900531	JP 88504505	A	19880526	199028	
US 4939732	A	19900703	US 88251212	A	19880714	199029	
KR 9201574	B1	19920218	WO 88JP508	A	19880526	199342	
			KR 89700166	A	19890130		
EP 315699	B1	19940302	EP 88904640	A	19880526	199409	
			WO 88JP508	A	19880526		
DE 3888091	G	19940407	DE 3888091	A	19880526	199415	
			EP 88904640	A	19880526		
			WO 88JP508	A	19880526		

Priority Applications (No Type Date): JP 87136784 A 19870529; ES 882960 A 19880929; JP 88504505 A 19880526

Cited Patents: 6.Jnl.Ref; EP 155882; GB 1144700; JP 55137742; JP 58165445; JP 59213006; JP 59228440; US 4144522; US 41445222

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 8809590	A	E	48		
Designated States (National): AU JP KR US					
Designated States (Regional): AT BE CH DE FR GB IT LU NL SE					
EP 315699	A	E			
Designated States (Regional): DE FR GB					
EP 315699	B1	E	25	H04L-001/00	Based on patent WO 8809590
Designated States (Regional): DE FR GB					
DE 3888091	G			H04L-001/00	Based on patent EP 315699
					Based on patent WO 8809590
KR 9201574	B1			H04L-001/00	

Abstract (Basic): WO 8809590 A

The error detecting method involves dummy codes being provided at a transmitter in a frame instead of the information signals if there is no information signal in the frame. Attribute flags are provided at the signal transmitter for informing attributions of the information signals and dummy codes. A check code is provided at the transmitter checking errors of attribute flags and information signals excluding attribute flags for the dummy codes and dummy codes.

A **second** check **code** is provided at the receiver by using received information signals, the dummy codes and attribute flags in the first frame. The **second** **code** checks errors of attribute flags and information signals, excluding attribute flags for the dummy codes and the dummy codes.

USE/ADVANTAGE - In oata processing system. System reduces re-transfer frequency of information signal due to errors occurring in dummy codes during serial transfer of information signal through line interface consisting of optical fibres. Quantity of information transfered is increased.

11/16

Title Terms: ERROR; CHECK; METHOD; SERIAL; TRANSFER; FORM; INFORMATION; SIGNAL; CYCLIC; REDUNDANT; CHECK; INFORMATION; SIGNAL; DUMMY; CODE; ATTRIBUTE; FLAG
Derwent Class: T01; U21; W01
International Patent Class (Main): H04L-001/00
International Patent Class (Additional): G06F-011/08; H03M-013/00; H04B-009/00; H04L-029/06
File Segment: EPI

17/5/10 (Item 10 from file: 350)

DIALOG(R)File 350:Derwent WPIX

007048847
WPI Acc No: 1987-048844/ **198707**
XRPX Acc No: N87-036991

Displacement-to-code converter - has unit of photoreceivers moving across scale with opaque and transparent sections to form code signals

Patent Assignee: MELNIK D I (MELN-I)
Inventor: MELNIK D I
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
SU 1239865	A	19860623	SU 3789480	A	19840912	198707	B

Priority Applications (No Type Date): SU 3789480 A 19840912
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
SU 1239865	A		5		

Abstract (Basic): SU 1239865 A

Accuracy of the converter is increased due to the introduction of a pulse generator, two counters, a register, three NAND-gates, a delay element, pulse shaper and **two** OR-gates. When the **code** scale is displaced relative to the block of photoreceivers by a value of its **period** t, the interaction of the active (transparent) and passive (opaque) parts produces 16 non-repeating correct code combinations. Inaccuracies in the manufacture of the scale and positioning of the photoreceivers can **produce** **erroneous** **code** **combinations** . These are corrected by use of Exclusive-OR-gates and an AND-gate to form the correct binary arithmetical code, and by counting the number of logic 1's on the inputs of a counter commutator. The signal from photoreceiver is then used to overcome failures associated with inaccurate manufacture of the scale, and errors in the positioning of photoreceivers.

USE/ADVANTAGE - Appts., may be used in digital measurement of linear and angular displacements of lathe servo parts, moving parts of instruments etc. Bul.23/23.6.86. (5pp Dwg.No.0/2

Title Terms: DISPLACEMENT; CODE; CONVERTER; UNIT; PHOTORECEIVER; MOVE; SCALE; OPAQUE; TRANSPARENT; SECTION; FORM; CODE; SIGNAL
Derwent Class: U21; W05
International Patent Class (Additional): H03M-001/26

File Segment: EPI

17/5/20 (Item 20 from file: 347)
DIALOG(R)File 347:JAPIO

04160832 **Image available**
CMOS SEMICONDUCTOR CIRCUIT

PUB. NO.: 05-152532 [JP 5152532 A]
PUBLISHED: June 18, 1993 (**19930618)**
INVENTOR(s): MURAKAMI KAZUO
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-361156 [JP 91361156]
FILED: November 27, 1991 (19911127)
INTL CLASS: [5] H01L-027/092
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD: R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, MOS)
JOURNAL: Section: E, Section No. 1441, Vol. 17, No. 542, Pg. 2, September 29, 1993 (19930929)

ABSTRACT

PURPOSE: To reduce an **erroneous operation** occurring at the **time** of **inputting** and outputting a signal between blocks in a CMOS semiconductor circuit in which a plurality of circuit blocks independently have power source lines and ground lines.

CONSTITUTION: A CMOS semiconductor circuit has a first circuit block 1b and a **second** circuit block 2b including independent power source potentials and ground potentials in such a manner that an output of the block 1b is inputted to the **second** block 2b, and comprises a circuit 3b for generating a potential of an intermediate of power source line potential of the first, **second** blocks or each ground line potential between input and output lines between the blocks 1b and 2b. Thus, an output potential level of the first block is matched with an **input** threshold value of the **second** block, and an **erroneous operation** occurring at the **time** of **inputting** /outputting a signal between the blocks is reduced.

17/5/21 (Item 21 from file: 347)
DIALOG(R)File 347:JAPIO

03836555 **Image available**
CAR SECURTITY SYSTEM

PUB. NO.: 04-201655 [JP 4201655 A]
PUBLISHED: July 22, 1992 (**19920722)**
INVENTOR(s): TEZUKA HIROYUKI
APPLICANT(s): KENWOOD CORP [000359] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-330566 [JP 90330566]
FILED: November 30, 1990 (19901130)
INTL CLASS: [5] B60R-025/10; G06F-015/00; G08B-015/00; H04Q-009/00; H04Q-009/00
JAPIO CLASS: 26.2 (TRANSPORTATION -- Motor Vehicles); 22.3 (MACHINERY -- Control & Regulation); 44.9 (COMMUNICATION -- Other); 45.4 (INFORMATION PROCESSING -- Computer Applications)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessers)
JOURNAL: Section: M, Section No. 1335, Vol. 16, No. 538, Pg. 102, November 09, 1992 (19921109)

ABSTRACT
PURPOSE: To prevent the **generation** of the drive mistake caused by the **erroneous operation** by varying the characteristic code level of the data including the characteristic ID code which is previously determined, in plural **times** and restricting the state which can be controlled according to the number of **times** of receiving and confirming the characteristic ID code on a body side.

CONSTITUTION: A remote controller 10 is equipped with a CPU 12 which receives signals from a switch 11 and starts operation, and when an operation starting signal is received from the switch 11, the CPU 12 sends out the characteristic ID code which is previously determined, to a modulation circuit 13 several **times** continuously. Accordingly, the data including the characteristic ID code is transmitted at lesst **two times**, varying each ID **code** level. After the signal received by the antenna 21 of a body 20 is received by a receiving circuit 22, and the signal is demodulated by a demodulation circuit 23, and supplied into a CPU 24. Accordingly, a prescribed control state operation among the control states is prohibited on the basis of the number of **times** of reception and confirmation of the received and demodulated ID code. Accordingly, the **generation** of the drive mistake caused by the **erroneous operation** can be prevented.

17/5/22 (Item 22 from file: 347)

03835108 **Image available**
AUTOMATIC TRAIN CONTROLLER

PUB. NO.: 04-200208 [JP 4200208 A]
PUBLISHED: July 21, 1992 (**19920721**)
INVENTOR(s): KOBAYASHI ZENICHIRO
SUMITA TOSHIKAZU
NARUTO MASASHI
IKEDA HIROAKI
APPLICANT(s): TEITO KOUSOKUDO KOUTSUU EIDAN [352191] (A Japanese Company or Corporation), JP (Japan)
MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-333284 [JP 90333284]
FILED: November 29, 1990 (19901129)
INTL CLASS: [5] B60L-015/40; B60L-003/00
JAPIO CLASS: 26.1 (TRANSPORTATION -- Railways); 22.3 (MACHINERY -- Control & Regulation); 37.2 (SAFETY -- Traffic); 43.4 (ELECTRIC POWER -- Applications)
JOURNAL: Section: M, Section No. 1333, Vol. 16, No. 531, Pg. 151, October 30, 1992 (19921030)

ABSTRACT
PURPOSE: To improve comfortableness and to realize anti-skid while enhancing operational efficiency by providing a **second** speed check section in addition to a first speed check section.

CONSTITUTION: A predetermined speed signal 6 is compared with a **second** limit speed signal 18 and when an actual speed exceeds a **second** limit speed, a **second** comparing circuit 12A produces a **command** 13 for interrupting a powering circuit and a normal maximum brake command 14. When the predetermined speed signal 6 exceeds a **second** limit speed signal 18 as well as a first limit speed signal 11 due to **erroneous** brake **operation** of an operator, the **second** comparing circuit 19 functions to **produce** the powering interruption command 13 and the normal maximum brake command 14 thus decelerating a train automatically. At that **time**, fluctuation of brake force is low as compared with a conventional system

and thereby comfortableness is not impaired and the probability of skid is very low.

17/5/23 (Item 23 from file: 347)
DIALOG(R)File 347:JAPIO

03507181 **Image available**
SATELLITE NAVIGATION RECEIVING DEVICE

PUB. NO.: 03-170081 [JP 3170081 A]
PUBLISHED: July 23, 1991 (**19910723)**
INVENTOR(s): ARAI OSAMU
MUNEMARU KIYOAKI
APPLICANT(s): FURUNO ELECTRIC CO LTD [368425] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-308362 [JP 89308362]
FILED: November 28, 1989 (19891128)
INTL CLASS: [5] G01S-005/14
JAPIO CLASS: 44.9 (COMMUNICATION -- Other); 34.4 (SPACE DEVELOPMENT -- Communication)
JAPIO KEYWORD:R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessers)
JOURNAL: Section: P, Section No. 1266, Vol. 15, No. 418, Pg. 71, October 23, 1991 (19911023)

ABSTRACT

PURPOSE: To extend and expand a **time** and a space where a position is measurable by **generating** a correct **dummy** noise **code** immediately after the switching point of a dummy noise code when the dummy noise code is switched at a constant **period** to track signals from plural satellites.

CONSTITUTION: **Two** C/A **code generators** 1 and 2 are used as a **dummy** noise **code generating** means and a switch 7 selects and supplies the outputs of **two** C/A **code** generators 1 and 2 to a reception part 3 alternately in order. A switch 6 selects a C/A code generator which generates a C/A code next **time** between the **two** C/A **code** generators 1 and 2. In this case, the C/A code outputted by the C/A code generator 1 is supplied to the reception part 3 in a state shown in a figure and data B is supplied to the C/A code generator **2** which generates a C/A **code** next. Then the data B is supplied and the C/A code corresponding to the data B can be outputted to the reception part 3 with a specified phase from right after the generator is switched to the side of the C/A code generator 2.

17/5/24 (Item 24 from file: 347)
DIALOG(R)File 347:JAPIO

03294848 **Image available**
SEMICONDUCTOR DEVICE

PUB. NO.: 02-270348 [JP 2270348 A]
PUBLISHED: November 05, 1990 (**19901105)**
INVENTOR(s): YASUE TADASHI
APPLICANT(s): SEIKO EPSON CORP [000236] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-091409 [JP 8991409]
FILED: April 11, 1989 (19890411)
INTL CLASS: [5] H01L-021/90
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, MOS)
JOURNAL: Section: E, Section No. 1025, Vol. 15, No. 26, Pg. 67,

January 22, 1991 (19910122)

ABSTRACT

PURPOSE: To prevent problems, such as the deterioration of the characteristics of a circuit due to the electrostatic coupling between elements or first wiring materials and a **second** wiring material, an **erroneous operation** and the like, from **generating** by a method wherein a grounded conductor film is provided between the elements or the first wiring materials formed on a substrate and a **second** wiring material formed on the elements or the first wiring materials through an insulating film.

CONSTITUTION: A grounded conductor film 9 is provided at least one part between elements or first wiring materials 6 formed on a substrate 1 and a **second** wiring material 8 formed on the elements or the materials 6 through an insulating film. For example, first wiring materials 6 are formed on a MOS transistor formed on a substrate 1, a conductor film 9 is formed through an insulating film 7 and moreover, a **second** wiring material 8 is formed through an insulating film 10. The film 9 is connected to a reference potential, such as a power line and the like. Thereby, problems, such as the deterioration of the characteristics of a circuit due to the electrostatic coupling between the elements or the materials 6 and the material 8, an **erroneous operation** and the like, are not **generated** and as the restraints of the arrangement of the material 2 are eliminated, an increase in the integration of a semiconductor device becomes possible.

17/5/25 (Item 25 from file: 347)

02933494

DISPLAY DEVICE

PUB. NO.: 01-231094 [JP 1231094 A]
PUBLISHED: September 14, 1989 (**19890914)**
INVENTOR(s): KAWAI TOSHIKATSU
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-056206 [JP 8856206]
FILED: March 11, 1988 (19880311)
INTL CLASS: [4] G09G-003/00
JAPIO CLASS: 44.9 (COMMUNICATION -- Other)
JOURNAL: Section: P, Section No. 973, Vol. 13, No. 554, Pg. 92, December 11, 1989 (19891211)

ABSTRACT

PURPOSE: To obtain a display device which is high in reliability and operating efficiency by receiving one-information **three** -sets of displaying **codes** from a host and fetching '2 out of 3' and then, displaying that transmission or a displaying code is faulty.

CONSTITUTION: This display device has a function which inputs displaying data from the outside in a consecutive sending from of three **times** per one **time** and when no omission exists in the code numbers given in the consecutive sending form, makes a majority logical discrimination. When an omission exists in the code numbers, the display device performs the majority logical discrimination after supplementing the omission by **producing** the **dummy code** number. When a result of majority logic is satisfied, the device displays displaying data corresponding to the code numbers, but, when the result does not satisfy, informs the outside of the fact. Moreover, when the code numbers of displaying data are not inputted from the outside within a previously fixed **time** , the display device discriminates that the input is discontinued due to the occurrence of abnormality and displays that the input discontinues. Therefore, any wrong display can be prevented by the majority logic of '2 out of 3' of input

data.

17/5/26 (Item 26 from file: 347)
DIALOG(R)File 347:JAPIO

02613052 **Image available**
SEQUENTIAL DECODER

PUB. NO.: 63-229952 [JP 63229952 A]
PUBLISHED: September 26, 1988 (**19880926**)
INVENTOR(s): SHIMODA KANEYASU
AGENO YUUZOU
KATO TADAYOSHI
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-062573 [JP 8762573]
FILED: March 19, 1987 (19870319)
INTL CLASS: [4] H04L-027/22; H03M-005/12
JAPIO CLASS: 44.3 (COMMUNICATION -- Telegraphy); 42.4 (ELECTRONICS -- Basic Circuits)
JOURNAL: Section: E, Section No. 707, Vol. 13, No. 31, Pg. 28, January 24, 1989 (19890124)

ABSTRACT

PURPOSE: To correctly decode a member code by providing a correction circuit for inverting or replacing demodulated data if a consecutive error takes place in a received code.

CONSTITUTION: If a sequential decoder 5 receives replaced or inverted data, since a received code stored in a buffer causes a **consecutive** erroneous **code** , a consecutive error detection circuit 6 measures the duration **time** of a skip signal **generated** to avoid **consecutively** erroneous **code** strings. If the duration **time** exceeds a predetermined **time** , a correction pattern in a correction circuit 4 provided to the input side of the sequential decoder 5 is switched by using an error signal sent from the consecutive error detection circuit 6 to replace or invert the demodulated data. Since the correction of the replacement or inversion of data is applied before the data is inputted to the sequential decoder **5** in this way, the member **code** is decoded correctly.

17/5/28 (Item 28 from file: 347)
DIALOG(R)File 347:JAPIO

02332658 **Image available**
METHOD FOR INPUTTING IMAGE INFORMATION

PUB. NO.: 62-249558 [JP 62249558 A]
PUBLISHED: October 30, 1987 (**19871030**)
INVENTOR(s): SHIJO KUNIO
APPLICANT(s): MATSUSHITA GRAPHIC COMMUN SYST INC [330729] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-093810 [JP 8693810]
FILED: April 23, 1986 (19860423)
INTL CLASS: [4] H04N-001/21
JAPIO CLASS: 44.7 (COMMUNICATION -- Facsimile)
JOURNAL: Section: E, Section No. 601, Vol. 12, No. 124, Pg. 93, April 16, 1988 (19880416)

ABSTRACT

PURPOSE: To eliminate a line memory and to extremely simplify the constitution of a circuit by inputting image information directly to a

memory controlled by a CPU bus.

CONSTITUTION: During the output of invalid data from a reading element 41, a CPU 40 executes a dummy instruction to adjust a **period** . After the execution of the instruction, the CPU 40 inputs effective image information outputted from the element 41 regularly and directly to the memory 43 controlled by the CPU BUS. At that **time** , the CPU 40 executes the **succeeding dummy instruction** to make the processing **time** , i.e., an **input period** Tb, coincide with the **time** required for shifting the image information in a shift register 50 by the bit width of a data bus 44. Consequently, the transfer **timing** of the image information outputted from a reading element control port 54 and the element 41 is synchronized with the input **timing** of the CPU 40 and the image information is directly inputted and stored to/in the memory 43 based on the synchronized **timing** .

17/5/30 (Item 30 from file: 347)
DIALOG(R)File 347:JAPIO

02066417 **Image available**
ABSOLUTE TYPE ENCODER

PUB. NO.: 61-280517 [JP 61280517 A]
PUBLISHED: December 11, 1986 (**19861211)**
INVENTOR(s): FUKAMIZU HIROSHI
TAKEDA IKUO
APPLICANT(s): OMRON TATEISI ELECTRONICS CO [000294] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 60-121955 [JP 85121955]
FILED: June 05, 1985 (19850605)
INTL CLASS: [4] G01D-005/249
JAPIO CLASS: 46.1 (INSTRUMENTATION -- Measurement)
JAPIO KEYWORD:R116 (ELECTRONIC MATERIALS -- Light Emitting Diodes, LED)
JOURNAL: Section: P, Section No. 574, Vol. 11, No. 144, Pg. 34, May 12, 1987 (19870512)

ABSTRACT

PURPOSE: To perfectly bring all of slit rows to a gray code system, by forming an additional code successively changing by one bit between adjacent non-gray codes at the **time** of non-gray between the mutual codes corresponding to adjacent slit rows.

CONSTITUTION: At the **time** of non-gray between a code 059 of an angle 359 deg. and a code 399 of an angle 000 deg., codes 0, 12, 9 of a dummy angle 359' and codes 3, 12, 9 of a dummy angle 000' are **inputted** . That is, the **dummy codes** 0, 12, 9 and 3, 12, 9 are determined so as to successively change by one bit between adjacent non-gray codes 059, 399 and all codes can be brought to a perfect gray code system by **two** gray forming additional **codes** . Therefore, even if the irregularity in the response speeds or level judging threshold values of a circuit system is present or there is a slight error in slit processing, no error is generated in an output signal.

17/5/32 (Item 32 from file: 347)
DIALOG(R)File 347:JAPIO

01833901 **Image available**
PROGRAMMABLE CONTROLLER

PUB. NO.: 61-048001 [JP 61048001 A]
PUBLISHED: March 08, 1986 (**19860308)**
INVENTOR(s): ISOBE MITSUNOBU

MATSUZAKI YOSHIE
OSAKO KAZUYOSHI
HATA SEIJI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 59-169316 [JP 84169316]
FILED: August 15, 1984 (19840815)
INTL CLASS: [4] G05B-019/02
JAPIO CLASS: 22.3 (MACHINERY -- Control & Regulation); 36.1 (LABOR SAVING DEVICES -- Industrial Robots)
JAPIO KEYWORD: R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, MOS); R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessers)
JOURNAL: Section: P, Section No. 478, Vol. 10, No. 206, Pg. 140, July 18, 1986 (19860718)

ABSTRACT

PURPOSE: To calculate various data while keeping the high speed characteristic of sequential controlling by switching, a general purpose microprocessor capable of system controlling and various data calculating with one-bit logical arithmetic processing without any overhead.

CONSTITUTION: A eneral purpose microprocessor MPU1 sets mode-switching flip- flop within a one-bit logical arithmetic processor LPU5 by the mode-switching instruction, and cuts off a program memory PM4 from a bus (c) to connect an operation code bus (d) with an instruction register LPU5, and an operand data bus (e) with an address bus (h), respectively, and the LPU5 is release from the holding condition. In the LPU mode, an MPU1 generates the address for the fetch of a logical arithmetic instruction IPU5 by the fetch of the first **dummy instruction** from a **dummy operation generator** 6 and the LPU5 is actuated by the fetch of the **second** dummy **instruction** to execute the arithmetic processing.

17/5/33 (Item 33 from file: 347)
DIALOG(R)File 347:JAPIO

01734645 **Image available**
SPREAD SPECTRUM COMMUNICATION SYSTEM

PUB. NO.: 60-213145 [JP 60213145 A]
PUBLISHED: October 25, 1985 (**19851025)**
INVENTOR(s): OGASAWARA MASAYUKI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 59-069760 [JP 8469760]
FILED: April 06, 1984 (19840406)
INTL CLASS: [4] H04J-013/00
JAPIO CLASS: 44.2 (COMMUNICATION -- Transmission Systems)
JOURNAL: Section: E, Section No. 387, Vol. 10, No. 61, Pg. 95, March 11, 1986 (19860311)

ABSTRACT

PURPOSE: To increase the change of detection of correlation on the receiving side and to shorten a synchronization confirmation **time** by applying redundancy to a false noise code of the longest code string at a degree preventing the randam property of a transmission side from damage.
CONSTITUTION: On the transmission side, a **false** noise **code** generating circuit **3** forms a **false** noise **code** in the longest code string and a code string 30 obtained by shifting the former code by 1/2 at its phase and an exclusive OR23 switches said codes successively in each code **period** to form a code string 31 having the **period** of twice the original code **period** and transmit data as a spread spectrum wave SS on the basis of the code string 31. On the receiving side, the same false noise code 32 as that of the transmission side and a code string 23 phase-shifted by 1/ **2** the

code **period** are inputted to two delay circuits 28, i.e. 1/2-bit and 1-bit delay circuits, and **two** **code** strings each of which consists of **three** kinds of **codes** are outputted from the circuits 28, properly selected by a switch circuit 29 and sent to three correlators 7-9. A synchronization detecting circuit 26 detects respective correlator output signals and also controls a clock signal control circuit 19 and a code string switching circuit 29 on the basis of output signals from pattern detectors 21, 25 outputting certain patterns in each code string **period** of a **false** noise **code** **generating** circuit 20.

17/5/35 **(Item 35 from file: 347)**
DIALOG(R)File 347:JAPIO

00710946 **Image available**
SPREAD SPECTRUM COMMUNICATION SYSTEM

PUB. NO.: 56-031246 [JP 56031246 A]
PUBLISHED: March 30, 1981 (**19810330)**
INVENTOR(s): TSUKAMOTO NOBUO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 54-107261 [JP 79107261]
FILED: August 24, 1979 (19790824)
INTL CLASS: [3] H04J-001/00
JAPIO CLASS: 44.2 (COMMUNICATION -- Transmission Systems)
JOURNAL: Section: E, Section No. 59, Vol. 05, No. 82, Pg. 155, May 29, 1981 (19810529)

ABSTRACT

PURPOSE: To shorten the synchronization establishing **time** in the search mode, by using two carrier waves different in frequency and **two** false noise **codes** different in **code** .

CONSTITUTION: Transmission data S17 and **false** signal **code** S16 are **added** by binary **adder** 3, and carrier wave S11 is phase-modulated by output S18 and is input to adder 16. Carrier wave S11 is input to phase modulator 14 and is modulated by false noise signal S13 and is **input** to **adder** 16. **False** signal noise **code** S13 is **input** to binary **adder** 13, and exclusive OR between this signal and start pulse S12 is operated to output polarity-inverted pulse S14. Carrier wave S10 is modulated in phase modulator 15 by this signal to output signal S15, and this signal is input to adder 16. These three kinds of signal are mixed and are output from antenna 8. Radio waves received by antenna 20 are separated by filter circuits 41 and 21 and are input to the phase modulator to take out frequency components S19 of the difference between outputs of circuits 41 and 21.

17/5/36 **(Item 36 from file: 347)**
DIALOG(R)File 347:JAPIO

00125383
REMOTE CONTROL SYSTEM

PUB. NO.: 52-084383 [JP 52084383 A]
PUBLISHED: July 13, 1977 (**19770713)**
INVENTOR(s): TSUBOI GIICHI
UTSU YOSHITOMO
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 50-158817 [JP 75158817]
FILED: December 29, 1975 (19751229)

INTL CLASS: [2] H04Q-009/00; H04Q-009/08; H04N-005/44
JAPIO CLASS: 22.3 (MACHINERY -- Control & Regulation); 44.6 (COMMUNICATION -- Television)
JAPIO KEYWORD: R007 (ULTRASONIC WAVES); R116 (ELECTRONIC MATERIALS -- Light Emitting Diodes, LED)
JOURNAL: Section: M, Section No. 47, Vol. 01, No. 141, Pg. 4993, November 17, 1977 (19771117)

ABSTRACT

PURPOSE: To make it possible to do the precise operation for preventing the erroneous action by noise or others by means that the remote control signal is made by **adding** the **second** frequency erroneous **action** preventing signal before and after or either one of the first frequency working pulse signal.

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File 275:Gale Group Computer DB(TM) 1983-2006/Mar 17
         (c) 2006 The Gale Group
File 621:Gale Group New Prod.Annou.(R) 1985-2006/Mar 17
         (c) 2006 The Gale Group
File 636:Gale Group Newsletter DB(TM) 1987-2006/Mar 17
         (c) 2006 The Gale Group
File  16:Gale Group PROMT(R) 1990-2006/Mar 20
         (c) 2006 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
File 148:Gale Group Trade & Industry DB 1976-2006/Mar 17
         (c)2006 The Gale Group
File 624:McGraw-Hill Publications 1985-2006/Mar 20
         (c) 2006 McGraw-Hill Co. Inc
File  15:ABI/Inform(R) 1971-2006/Mar 20
         (c) 2006 ProQuest Info&Learning
File 647:CMP  Computer Fulltext 1988-2006/Apr W2
         (c) 2006 CMP Media, LLC
File 674:Computer News Fulltext 1989-2006/Mar W2
         (c) 2006 IDG Communications
File 696:DIALOG Telecom. Newsletters 1995-2006/Mar 17
         (c) 2006 Dialog
File 369:New Scientist 1994-2006/Aug W4
         (c) 2006 Reed Business Information Ltd.
File 810:Business Wire 1986-1999/Feb 28
         (c) 1999 Business Wire
File 813:PR Newswire 1987-1999/Apr 30
         (c) 1999 PR Newswire Association Inc
File 610:Business Wire 1999-2006/Mar 20
         (c) 2006 Business Wire.
File 613:PR Newswire 1999-2006/Mar 20
         (c) 2006 PR Newswire Association Inc

Set     Items   Description
S1       3876   (DUMMY OR FAKE OR FALSE OR GARBAGE OR NONSENSE OR JUNK OR -
             RUBBISH OR BOGUS OR PHONY OR MOCK OR MISLEADING OR ERRONEOUS -
             OR AMBIGUOUS OR USELESS)(2W)(INSTRUCTION? ? OR OPERATION? ? OR
              COMMAND? ? OR CODE? ? OR ACTION? ? OR TASK? ?)
S2       1841   (DUMMY OR FAKE OR FALSE OR GARBAGE OR NONSENSE OR JUNK OR -
             RUBBISH OR BOGUS OR PHONY OR MOCK OR MISLEADING OR ERRONEOUS -
             OR AMBIGUOUS OR USELESS)(2W)(JOB? ? OR TRANSACTION? ? OR CODE-
             WORD? ?)
S3        752   (PHONEY OR INVALID)(2W)(INSTRUCTION? ? OR OPERATION? ? OR -
             COMMAND? ? OR CODE? ? OR ACTION? ? OR TASK? ? OR JOB? ? OR TR-
             ANSACTION? ?)
S4        899   S1:S3(10N)(INTRODUC? OR INPUT???? OR ADD??? OR INSERT??? OR
              ENTER??? OR GENERAT??? OR CREAT??? OR MIX??? OR INTERLEAV???
             OR COMBIN? OR MERG??? OR SLOT???? OR INCORPORAT? OR PRODUC????
              OR INTERSPERS? OR INTERMINGL???)
S5         38   S1:S3(10N)(INTEGRAT? OR MIX??? OR INTERMIX??? OR SPRINKL??-
             ?)
S6     115610   (USEFUL OR FUNCTIONAL OR PROPER OR CORRECT OR NORMAL OR RE-
             GULAR OR RIGHT OR ACTIVE OR VALID OR LEGITIMATE)(2W)(INSTRUCT-
             ION? ? OR OPERATION? ? OR COMMAND? ? OR CODE? ? OR ACTION? ? -
             OR TASK? ? OR JOB? ? OR TRANSACTION? ?)
S7       2882   (SUCCEEDING OR SUCCESSIVE OR CONSECUTIV? OR ENSUING OR TWO
             OR SECOND??? OR SAME OR EQUAL OR IDENTICAL OR THREE OR THIRD -
             OR FOUR OR FOURTH OR FIVE OR FIFTH OR NUMBER OR AMOUNT)(5W)S6
S8   19586895   TIME? ? OR TIMING OR INTERVAL? ? OR PERIOD? ? OR SECOND? ?
             OR MINUTE? ? OR HOUR? ?
S9          3   S4:S5(100N)S7(100N)S8
S10         3   S4:S5(100N)S7
S11    383512   (SUCCEEDING OR SUCCESSIVE OR CONSECUTIV? OR ENSUING OR TWO
             OR SECOND??? OR SAME OR EQUAL OR IDENTICAL OR NUMBER OR AMOUN-
             T)(5W)(INSTRUCTION? ? OR OPERATION? ? OR COMMAND? ? OR CODE? ?
```

```
            OR ACTION? ? OR TASK? ?)
S12     245743   (THREE OR THIRD OR FOUR OR FOURTH OR FIVE OR FIFTH)(5W)(IN-
           STRUCTION? ? OR OPERATION? ? OR COMMAND? ? OR CODE? ? OR ACTI-
           ON? ? OR TASK? ?)
S13         26   S4:S5(50N)S11:S12(50N)S8
S14         26   S9:S10 OR S13
S15         23   RD  (unique items)
S16         19   S15 NOT PY=2000:2006
```

16/3,K/1 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01614393 SUPPLIER NUMBER: 14193051 (USE FORMAT 7 OR 9 FOR FULL TEXT)
The processor war. (DEC AXP PC, Intel Pentium and Apple-IBM-Motorola PowerPC microprocessors compete for desktop market)
Mayfield, Michael; Feniello, Mark
DEC Professional, v12, n8, p50(2)
August, 1993
ISSN: 0744-9216 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 1183 LINE COUNT: 00091

... pipeline. The use of multiple pipelines allows several entire streams of instructions to execute at the same **time** . Both the AXP PC and Pentium have separate integer and floating-point pipelines, plus separate branch-prediction...

...any type of integer or logical operation. The other integer pipeline can handle only "simple" instructions. This **second** pipeline allows many common **instructions** to be handled in parallel without introducing the complications required to implement two full-featured piplines. Given the **proper** mix of **instructions** , Pentium can execute **two** integer **instructions** per cycle, in contrast with one for the AXP PC.
This parallelism can greatly improve performance over...
...for example, the following C code segment:
for (k=i+prime; k<SIZE: k+=prime)
flags[k] = **FALSE**
This **code** would **generate** the following assembly language instructions for the main body of the loop:
100 p
mov byte ptr...

...Repeat loop while k(SIZE
Each execution of this loop requires six cycles on the 486. The **same code** requires only two cycles on the Pentium, one for the mov and add together and one for...

16/3,K/2 (Item 2 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01597788 SUPPLIER NUMBER: 13782231 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Windows NT virtual device drivers for hardware-dependent 16-bit applications. (Microsoft Windows NT operating system) (includes related articles on virtual device driver interface and Windows NT registration database) (Technical)
Tomlinson, Paula
Windows-DOS Developer's Journal, v4, n5, p6(14)
May, 1993
DOCUMENT TYPE: Technical ISSN: 1059-2407 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 4992 LINE COUNT: 00387

... and what values to load into the registers before it returns. And, of course, since it has **added four** bytes of **nonsense** to your **code** , it has to increment the instruction pointer past those bytes. Upon return from the exception handler, your...

...that first appeared in Windows 3.1 contained information only for SHELL and OLE applications. At that **time** , Microsoft introduced an API for querying and setting values in the registration database. In Win32, the new ...

16/3,K/3 (Item 3 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01444900 SUPPLIER NUMBER: 11099457 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Target practice. (Software Review) (Symantec Corp.'s On Target project management software) (evaluation)
Williams, Iwan
PC User, n163, p65(1)
July 17, 1991
DOCUMENT TYPE: evaluation ISSN: 0263-5720 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 616 LINE COUNT: 00050

... way tasks can be linked is end-to-start and the absence of a provision to start **two tasks** at the same **time** means that you might have to **create dummy tasks** as a workaround.
A project can also be displayed in a Work Flow window -- as a PERT...

...groups of tasks. Graphs indicating resource loading and costs can be added to the bottom of the **Time** Table.
Any On Target window can be expored to a word processor document via the Windows Clipboard...

16/3,K/4 (Item 4 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01437338 SUPPLIER NUMBER: 10881310 (USE FORMAT 7 OR 9 FOR FULL TEXT)
The art of reverse engineering. (tutorial)
Swanke, Robert S.
Computer Language, v8, n6, p57(4)
June, 1991
DOCUMENT TYPE: tutorial ISSN: 0749-2839 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 1229 LINE COUNT: 00105

... a disassembler is an assembly listing that may not be 1 00% accurate. For example, should an **ambiguous** line of **code** be rendered as MOV BX,100 or MOV BX, OFFSET **addr** ?
After you've run a program through an automated disassembler, I suggest the following **time** -consuming steps to make the listing perfect.
First, examine all code/data boundaries to ensure no code...

...as this sequence: MOV CX, 123 ; Change CH MOV CH,O ; Again XOR CX,CX ; And again
Second , examine all segment register **operations** to ensure that subsequent data addressing is correct: MOV BX,40 MOV ES,BX MOV ES: INT05...

16/3,K/5 (Item 5 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01419591 SUPPLIER NUMBER: 10364234 (USE FORMAT 7 OR 9 FOR FULL TEXT)
An elementary C cost model. (estimating the cost of operations on a computer in the C programming language) (tutorial)
Bentley, Jon; Kernighan, Brian; Van Wyk, Chris
UNIX Review, v9, n2, p38(9)
Feb, 1991
DOCUMENT TYPE: tutorial ISSN: 0742-3136 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 2620 LINE COUNT: 00201

... page 46. For each operation, we see the cost of five experiments measured in the basic system **time** unit of "clicks" (1/60th of a **second** on this machine), followed by the average cost in microseconds.
The first dozen lines give us access to the system **timing** routines. This is the part of the program that varies most from system to system-the **time** function gives less accurate **times** but is more portable. The middle part of the program contains the two macros that are the heart of the **timing** experiment: loop1 runs a single experiment, while loop performs a group of **five** and prints out the **operation** name and average cost. These are macros rather than functions because we pass executable code to them...
...average number of microseconds taken by the null loop is subtracted from later operations (but the raw **time** in clicks is still printed). Some changes are cosmetic. Some changes are invisible: we **added** some " **dummy** " **operations** between the inner loops in an attempt to avoid identical cache alignments. We also added a simple...

16/3,K/6 (Item 6 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01380486 SUPPLIER NUMBER: 09606063 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Learning Windows Part III: control windows and MDI support. (Multiple Document Interface) (tutorial)
Adler, Marc
Microsoft Systems Journal, v5, n6, p67(19)
Nov, 1990
DOCUMENT TYPE: tutorial ISSN: 0889-9932 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 7410 LINE COUNT: 00565

... a nonzero value, the keystroke was translated.
if (!TranslateMDISysAccel(hwndMDIClient, &msg) &&
!TranslateAccelerator(hWndMain, hAccelTable, &msg))
The second **change** was registering a window class for the MDI child windows. Nothing in this code reveals that these...

...GRAPH)); wc.lpszMenuName = NULL; wc.cbWndExtra = CBWNDEXTRA;
wc.lpszClassName = "GraphWindow"; if (!RegisterClass(&wc)) { return FALSE;
}
The third **task** **was** creating **the** MDI client window. This needs to be done when the main window is created. An easy way...

16/3,K/7 (Item 7 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01358156 SUPPLIER NUMBER: 08407480 (USE FORMAT 7 OR 9 FOR FULL TEXT)
An income and expense recorder. (using Lotus 1-2-3 to manage business balance sheets) (tutorial)
Nelson, Stephen L.
Lotus, v6, n5, p52(4)
May, 1990
DOCUMENT TYPE: tutorial ISSN: 8756-7334 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 1781 LINE COUNT: 00133

... the description of a new record.
If you're finished entering records, press Return. The macro uses **two** Data Table **commands** to calculate the totals for each of the income and expense catagories shown in figure 1. The first Data Table command calculates income categories; the **second** calculates expense categories. The macro then recalculates the entire worksheet and returnes you to cell

A1.
Unfortunately...in Release 3. However, unless you've constructed a massive database, it should take only a few **seconds** to calculate. If speed of recalculation becomes a problem in Release 3, see the Help/3 column on page 24.
STEP 3. Review for mistakes and correct them. The macro prevents you from **entering invalid codes** or amounts, but it can't tell if you mistype an amount or mix up category names...

16/3,K/8 (Item 8 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01299806 SUPPLIER NUMBER: 07330266 (USE FORMAT 7 OR 9 FOR FULL TEXT)
A new check register. (using a macro to balance a checkbook) (Lotus Development Corp.'s Lotus 1-2-3 spreadsheet software)
Nelson, Stephen L.
Lotus, v5, n6, p36(7)
June, 1989
ISSN: 8756-7334 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 2285 LINE COUNT: 00169

... year,month,day) formula. For example, @DATE(89,6,3) returns 03-Jun-89. Num Enter corrected **number** or **code** (DEP, WD, or ATM) as a right-aligned label--for example, "104. Amount Enter a deposit as...edit this field. Ctg Enter category code as an uppercase, right-aligned label--for example, "FOOD. Description **Enter** new description text.
Regarding the **second** case--a completely **erroneous transaction** --you must manually **enter** a correct, substitute transaction in place of the **erroneous transaction** . Warning: Do not use the Worksheet Delete Row command to delete the row containing the erroneous transaction...

16/3,K/9 (Item 9 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01103603 SUPPLIER NUMBER: 00576122 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Project Management with the PC.
Edwards, K.
PC Magazine, v3, n21, p109-117
Oct. 30, 1984
DOCUMENT TYPE: evaluaton ISSN: 0888-8507 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 15928 LINE COUNT: 01208

... over for me.
A thorough examination of the case study network chart revealed nine "dangling" nodes. I **created dummy tasks** to link these to the first or last node in the network (to eliminate the possibility that these dummy tasks might affect the critical path) and tried again. This **time** EX-PERT/80 took just over 1 **minute** to solve for the 94 tasks (85 original and 9 dummy tasks). The task list took 2 **minutes** to print, and the Gantt chart took 6-1/2 **minutes** (and six sheets of paper).
It was a simple matter to remove the required task from the list and solve the problem (1 **minute** and 14 **seconds**), and then replace kthe **task** and solve again (1 **minute** and 14 **seconds**). The critical path and project completion times were the same at the start and finish of the...

16/3,K/10 (Item 1 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)

01189963 Supplier Number: 42903833 (USE FORMAT 7 FOR FULLTEXT)
ROLM INCREASES FOCUS ON SYSTEM SECURITY WITH NEW OFFERING
News Release, p1
April 10, 1992
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 654

... to help customers
limit their number of authorized Direct Inward System Access (DISA) users, thereby limiting the **number** of **valid codes** hackers could discover. Also, a DISA caller is now dropped after a single attempt to **enter** a system using an **invalid code** .

In September 1991, ROLM announced several terminal port security enhancements, including:

- Engineering passwords and formats changed with...

...passwords on a
customer-configurable basis;

- Automatic logoff if a system is idle for a customer-determined **period** of **time** .

LeeMah DataCom Security is located in Hayward, CA., and is a wholly owned subsidiary of LeeMah Electronics...

16/3,K/11 (Item 1 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2006 The Gale Group. All rts. reserv.

11225172 SUPPLIER NUMBER: 55306275 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Firm strategy and age dependence: a contingent view of the liabilities of newness, adolescence, and obsolescence.
Henderson, Andrew D.
Administrative Science Quarterly, 44, 2, 281(3)
June, 1999
ISSN: 0001-8392 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 16305 LINE COUNT: 01420

... standards-based strategies represent two fundamentally different strategic gestalts (cf. Miller and Friesen, 1980) that were seldom **mixed** . Given this, strategy was represented by a **dummy** variable, **coded** 1 if a firm derived at least 50 percent of its sales from proprietary technology in the...

...percent of the firms maintained the same strategy throughout their lives. Thus, even though strategy was not **time** -varying, it accurately represented the behavior of most firms. To account for the few firms that did change strategy, I used **two** controls. Changed strategy was **coded** 1 beginning in the year that a firm's sales switched to or from a proprietary majority...

16/3,K/12 (Item 2 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2006 The Gale Group. All rts. reserv.

10915293 SUPPLIER NUMBER: 54260432 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Self-generated power locks.(Cover Story)
Rose, Thomas B.
Doors and Hardware, 63, 3, 20(3)
March, 1999

DOCUMENT TYPE: Cover Story ISSN: 0361-5294 LANGUAGE: English
RECORD TYPE: Fulltext
WORD COUNT: 1533 LINE COUNT: 00118

... s ID right there at the lock. The user can then select his/her own personal identification **number** to complete the user access **code** .
Can a self-powered lock protect against someone trying to randomly access the lock? As with other...

...control locks, self-powered locks have a "wrong try lockout." At the owner's choice, when between **three** and nine **invalid** access **codes** have been **entered** , the lock will not accept any code for between 0 and 90 **seconds** , programmable, from the last attempt. As with all other transactions, lights and beeps will signify when the lock is in lockout and when the lockout **period** expires. This activity will show up on the audit record to alert management that unauthorized entry has...

16/3,K/13 (Item 3 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2006 The Gale Group. All rts. reserv.

06432871 SUPPLIER NUMBER: 13689982 (USE FORMAT 7 OR 9 FOR FULL TEXT)
A predictive validation study of the methods used to select eligibility technicians.
Cesare, Steven J.; Blankenship, Mark H.; Giannetto, Patrick W.; Mandel, Mark Z.
Public Personnel Management, v22, n1, p107(16)
Spring, 1993
ISSN: 0091-0260 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 5843 LINE COUNT: 00503

... variable and applicant ethnicity and gender as the independent variables.
The six ethnic classifications were coded as **five** dummy- **coded** vectors with the Filipino classification being coded as zero on all **five** vectors. These **five** **dummy** - **coded** vectors were **entered** into the regression equation as a block on the first step. The change in |R.sup.2
was used to examine the main effect for the six ethnic groups. Next, the **two** gender classifications were **coded** as one dummy-coded vector with the female condition being coded as zero on that vector. This vector was entered into the regression equation on the **second** step of the analysis and represents the main effect for applicant gender. This change in |R.sup...

...the effects due to applicant ethnicity (Cohen & Cohen, 1983). Finally, the five vectors formed from the cross **products** of the **dummy** - **coded** vectors, for ethnicity and gender, were **entered** as the final step of the hierarchical regression analysis. Changes in |R.sup.2
as a result...

16/3,K/14 (Item 4 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2006 The Gale Group. All rts. reserv.

06095117 SUPPLIER NUMBER: 12477635 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Keypad component for customizing: custom security includes a thorough knowledge of each component, including keypads. (see related articles on keypad options and selling)
Schum, John L.
Doors and Hardware, v56, n8, p34(5)
July, 1992
ISSN: 0361-5294 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 2332 LINE COUNT: 00183

... or remote alarm that tampering is in progress. Features commonly available to discourage unauthorized access include:
* Large **number** of combinations - allows frequent **code** changes. This
especially frustrates a perpetrator from trying all possible codes over a period
of time.
* Error...

...if a
wrong code is entered. This prevents someone from trying multiple codes
in a short time **period** .
* Code entry **time** - the system allows a set **amount** of **time** to enter the
code and then resets. Anyone taking an excessive amount of **time** is probably
guessing at the correct code.
* Error detection - usually a **timed** local alarm if **two** or **three** **invalid**
codes are **entered** in succession. The alarm usually discourages someone
from spending much **time** trying to hit the correct code.
The Input
Every electronic device needs input power. Most keypads require...

...a code to use to request entry. Output signal is sent to a remote receiver
Code Entry **Time** : The **time** allowed for code entry before reset takes place
Display: A liquid crystal display showing system status and/or other information
Door Prop: The length of **time** a door can be unlocked and held open before an alarm sounds. Usually programmable and may require...

...initiate access. Output signal is sent a remote, monitored receiver
Error Detection: Local or remote alarm if **two** or **three** **invalid** **codes** are **entered** in succession
Error Lockout: Inactive **time** **period** after a wrong code entry
Illumination: Background lamp or lighted digits for nighttime or unlighted areas
Indicators...

...for "slim line" mounting for door frames, surface and flush mounting, weatherproofing and spy-proofing housings
Multiple **Time** Zones: Programming to

16/3,K/15 (Item 5 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

05123702 SUPPLIER NUMBER: 10408035 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Answering the need for WORM and rewritable optical storage: the Pioneer multifunction optical disk drive. (write once, read many times)
Ekberg, Kent F.; Millet, Richard; Simpson, Cris
Optical Information Systems, v11, n1, p19(5)
Jan-Feb, 1991
ISSN: 0886-5809 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 2875 LINE COUNT: 00225

... drive has an embedded SCSI controller and a single internal SCSI connector. The external drive subsystem has **two** SCSI connectors for daisy chain **operation** .

The multifunction optical disk drive has **two** different modes of **operation** : rewritable and WORM. The default mode is set at start-up by a dip switch, but the mode may be changed at any **time** under software control. In WORM mode, the drive emulates a Pioneer DD-5001 series drive down to...

...mode, the ERASE operate without modification. In WORM mode, the ERASE and FORMAT commands will cause an **INVALID COMMANd** error. To handle the various modes, Pioneer **introduced**
the vendor unique

16/3,K/16 (Item 6 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

04505873 SUPPLIER NUMBER: 08107362 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Flash ADCs provide the basis for high-speed conversion. (analog-to-digital converters)(part 1)
Kester, Walt
EDN, v35, n1, p101(8)
Jan 4, 1990
ISSN: 0012-7515 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 3439 LINE COUNT: 00276

... with a reference voltage above the level of the input signal will produce a logic 0. A **secondary** logic stage decodes the thermometer **code** that results from the [2.sub.2]-1 comparisons. An optional output register latches the decoding stage's digital output for one clock cycle.
Timing is everything
One of the first difficulties you'll encounter when using flash converters is removing valid...

...the clock command. When this signal is in its convert-command state, the comparators track the analog- **input** signal, and during this **time** the output data is **invalid** . When the **command** line changes state, it latches the comparator outputs. Valid output data is now available for transfer to ...

16/3,K/17 (Item 1 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)

01760070 04-11061
Effects of realistic job previews on multiple organizational outcomes: A meta-analysis
Phillips, Jean M
Academy of Management Journal v41n6 PP: 673-690 Dec 1998
ISSN: 0001-4273 JRNL CODE: AMA
WORD COUNT: 11164

...TEXT: of effect sizes.

To determine the unique contribution of each set of moderator variables (RJP setting, RJP **timing** , and RJP medium), I conducted a weighted least squares regression analysis for each outcome variable. The outcome variable was regressed on the **three** sets of **dummy** - **coded** moderators, each **entered** as a block. Table 3 presents the results of the moderator analyses. The order of entry for...

...field setting was the first variable to impact the study participant, so setting was entered first. The **timing** of the RJP would next impact the participant, so **timing** was entered **second** , followed by the medium of the RJP. As shown in Table 3, all but one (setting moderating...

16/3,K/18 (Item 2 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)

01439592 00-90579
WLL: Some reasons to believe
Sweeney, Dan
Cellular Business v14n6 PP: 26-30 Jun 1997
ISSN: 0741-6520 JRNL CODE: CLB
WORD COUNT: 1811

...TEXT: between codes. Such orthoganal coding involves the synchronization of all transmissions in the network to prevent the **generation** of **false codes** resulting from **timing** errors. It is supposed to reduce the carrier-to-noise constraints of non-orthogonal CDMA systems thereby permitting simultaneous transmissions equaling near the **number** of available **codes** .

WLL is so new and still so provisional that assessing the claims made for any of these...

16/3,K/19 (Item 3 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)

01420246 00-71233
The effect of national culture, organizational complementarity, and economic motivation on joint venture dissolution
Park, Seung Ho; Ungson, Gerardo R
Academy of Management Journal v40n2 PP: 279-307 Apr 1997
ISSN: 0001-4273 JRNL CODE: AMA
WORD COUNT: 11779

...TEXT: stable than ventures that target domestic (in one or both partners' countries) markets or involve a single **product** or project. We used **two dummy** variables, respectively **coded** 1 when a joint venture targeted markets in multiple countries or involved multiple products or projects. We...

...were selected.

Data Analysis

Event-history analysis was used because it is uniquely suited to studying a **time** series of discrete events for right-censored data: cases for which an event has not occurred by the end of the study **period** are also amenable to analysis. The unit of analysis was a joint venture, and an event was...

```
File   8:Ei Compendex(R) 1970-2006/Mar W2
         (c) 2006 Elsevier Eng.  Info. Inc.
File  35:Dissertation Abs Online 1861-2006/Feb
         (c) 2006 ProQuest Info&Learning
File  65:Inside Conferences 1993-2006/Mar 20
         (c) 2006 BLDSC all rts. reserv.
File   2:INSPEC 1898-2006/Mar W2
         (c) 2006 Institution of Electrical Engineers
File  94:JICST-EPlus 1985-2006/Dec W4
         (c)2006 Japan Science and Tech Corp(JST)
File   6:NTIS 1964-2006/Mar W1
         (c) 2006 NTIS, Intl Cpyrght All Rights Res
File 144:Pascal 1973-2006/Feb W4
         (c) 2006 INIST/CNRS
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File  34:SciSearch(R) Cited Ref Sci 1990-2006/Mar W2
         (c) 2006 Inst for Sci Info
File  99:Wilson Appl. Sci & Tech Abs 1983-2006/Feb
         (c) 2006 The HW Wilson Co.
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         Comp & dist by NTIS, Intl Copyright All Rights Res
File  95:TEME-Technology & Management 1989-2006/Mar W2
         (c) 2006 FIZ TECHNIK

Set     Items   Description
S1       1816   (DUMMY OR FAKE OR FALSE OR GARBAGE OR NONSENSE OR JUNK OR -
             RUBBISH OR BOGUS OR PHONY OR MOCK OR MISLEADING OR ERRONEOUS -
             OR AMBIGUOUS OR USELESS)(2W)(INSTRUCTION? ? OR OPERATION? ? OR
              COMMAND? ? OR CODE? ? OR ACTION? ? OR TASK? ?)
S2        109   (DUMMY OR FAKE OR FALSE OR GARBAGE OR NONSENSE OR JUNK OR -
             RUBBISH OR BOGUS OR PHONY OR MOCK OR MISLEADING OR ERRONEOUS -
             OR AMBIGUOUS OR USELESS)(2W)(JOB? ? OR TRANSACTION? ? OR CODE-
             WORD? ?)
S3         73   (PHONEY OR INVALID)(2W)(INSTRUCTION? ? OR OPERATION? ? OR -
             COMMAND? ? OR CODE? ? OR ACTION? ? OR TASK? ? OR JOB? ? OR TR-
             ANSACTION? ?)
S4        250   S1:S3(10N)(INTRODUC? OR INPUT???? OR ADD??? OR INSERT??? OR
              ENTER??? OR GENERAT??? OR CREAT??? OR MIX??? OR INTERLEAV???
             OR COMBIN? OR MERG??? OR SLOT???? OR INCORPORAT? OR PRODUC????
              OR INTERSPERS? OR INTERMINGL???)
S5         12   S1:S3(10N)(INTEGRAT? OR MIX??? OR INTERMIX??? OR SPRINKL??-
             ?)
S6      47767   (USEFUL OR FUNCTIONAL OR PROPER OR CORRECT OR NORMAL OR RE-
             GULAR OR RIGHT OR ACTIVE OR VALID OR LEGITIMATE)(2W)(INSTRUCT-
             ION? ? OR OPERATION? ? OR COMMAND? ? OR CODE? ? OR ACTION? ? -
             OR TASK? ? OR JOB? ? OR TRANSACTION? ?)
S7       1272   (SUCCEEDING OR SUCCESSIVE OR CONSECUTIV? OR ENSUING OR TWO
             OR SECOND??? OR SAME OR EQUAL OR IDENTICAL OR THREE OR THIRD -
             OR FOUR OR FOURTH OR FIVE OR FIFTH OR NUMBER OR AMOUNT)(5W)S6
S8   11024412   TIME? ? OR TIMING OR INTERVAL? ? OR PERIOD? ? OR SECOND? ?
             OR MINUTE? ? OR HOUR? ?
S9          0   S4:S5 AND S7 AND S8
S10         0   S4:S5 AND S7
S11         8   S4:S5 AND S6
S12       122   S4:S5 AND S8
S13    160744   (SUCCEEDING OR SUCCESSIVE OR CONSECUTIV? OR ENSUING OR TWO
             OR SECOND??? OR SAME OR EQUAL OR IDENTICAL OR NUMBER OR AMOUN-
             T)(5W)(INSTRUCTION? ? OR OPERATION? ? OR COMMAND? ? OR CODE? ?
              OR ACTION? ? OR TASK? ?)
S14     68432   (THREE OR THIRD OR FOUR OR FOURTH OR FIVE OR FIFTH)(5W)(IN-
             STRUCTION? ? OR OPERATION? ? OR COMMAND? ? OR CODE? ? OR ACTI-
             ON? ? OR TASK? ?)
S15        14   S12 AND S13:S14
S16        22   S11 OR S15
```

```
S17         17   RD  (unique items)
S18         12   S17 NOT PY=2000:2006
```

18/5/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03501338 E.I. Monthly No: EIM9210-053379
Title: Neural networks for digital adder.
Author: Morisue, M.; Sakai, K.; Iizuka, T.
Conference Title: 1991 IEEE International Symposium on Circuits and Systems Part 3 (of 5)
Conference Location: Singapore, Singapore Conference Date: 19910611
Sponsor: IEEE Circuits & Systems Soc
E.I. Conference No.: 16930
Source: Proceedings - IEEE International Symposium on Circuits and Systems v 3. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA (IEEE cat n 91CH3006-4). p 1605-1608
Publication Year: 1991
CODEN: PICSDI ISSN: 0271-4310
Language: English
Document Type: PA; (Conference Paper) Treatment: T; (Theoretical); A; (Applications)
Journal Announcement: 9210
Abstract: A description is presented of a binary **adder** using the Hopfield type neural network in which **false operations** due to local minimum equilibria are avoided. Emphasis is placed on the procedure to **correct** the **false operations** by **introducing** stable conditions of a neuron cell. In addition to this binary adder, the Hopfield type adder with a carry-look-ahead circuit is described. Furthermore, how the proposed adder is constructed using CMOS inverter is described. The simulation results show that the proposed adder can perform a high performance operation because of an almost constant operation time, regardless of increasing of the number of bits in the circuit. 2 Refs.
Descriptors: *NEURAL NETWORKS--*Applications; COMPUTER SIMULATION; INTEGRATED CIRCUITS, CMOS; COMPUTERS, DIGITAL--Adders
Identifiers: BINARY ADDERS; HOPFIELD NETWORKS; CMOS INVERTERS; CARRY-LOOKAHEAD CIRCUITS
Classification Codes:
723 (Computer Software); 721 (Computer Circuits & Logic Elements); 713 (Electronic Circuits)
72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS)

18/5/5 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

07039229 INSPEC Abstract Number: C9811-6130S-044
Title: A tentative approach to constructing tamper-resistant software
Author(s): Mambo, M.; Murayama, T.; Okamoto, E.
Author Affiliation: Sch. of Inf. Sci., Japan Adv. Inst. of Sci. & Technol., Ishikawa, Japan
Conference Title: New Security Paradigms Workshop. Proceedings p.23-33
Publisher: ACM, New York, NY, USA
Publication Date: 1998 Country of Publication: USA vi+116 pp.
ISBN: 0 89791 986 6 Material Identity Number: XX97-02034
U.S. Copyright Clearance Center Code: 0 89791 986 6/97/9..$5.00
Conference Title: Proceedings of Meeting on New Security Paradigms
Conference Sponsor: ACM; U.S. Dept. Defense; Univ. Newcastle upon Tyne
Conference Date: 23-26 Sept. 1997 Conference Location: Langdale, UK
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: So far tamper-resistance has been considered as a property where information stored in a device is hard to read or modify by tampering. Such tamper-resistance is quite important in many situations: superdistribution, electronic commerce systems using IC cards, pay television systems with decoders containing secret values for descrambling

images, and so on. Tamper-resistance ensures **proper operation** of a program and prevents extraction of secret data and abuse of the program. Moreover, tamper-resistance enables a vendor to enforce his own conditions upon users. A new notion of tamper-resistance is stated as follows. Tamper-resistance means that a property such as information stored in a device or software is hard to read or modify by tampering. A tamper-resistant device is usually expensive and not easy to handle compared with its realization in software. It is better to achieve tamper-resistance without relying on any physical device. Meanwhile, intellectual property rights for a software program can be easily violated once an attacker analyzes the algorithm of a target program. The attacker can create a distinct program which looks quite different but functions just as the target program does. It is very important for software programs to be protected from any reverse engineering and manipulation. From these observations we study methods to generate a tamper-resistant code and explain an elementary tool, a0/f1/f2/f3. It replaces and shuffles operational codes or **inserts** reproductive **dummy codes** in a program so that the output becomes hard to read. (11 Refs)
Subfile: C
Descriptors: industrial property; security of data; software engineering
Identifiers: tamper-resistant software development; superdistribution; electronic commerce; IC cards; pay television; intellectual property; reverse engineering; software tool
Class Codes: C6130S (Data security); C6110B (Software engineering techniques)

18/5/7 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

05252536 INSPEC Abstract Number: B9211-1265B-059, C9211-5230-014
Title: Simulation of neural network digital adder and multiplier
Author(s): Sakai, K.; Morisue, M.; Koinuma, H.
Author Affiliation: Fac. of Eng., Saitama Univ., Urawa, Japan
Journal: Electronics and Communications in Japan, Part 3 (Fundamental Electronic Science) vol.75, no.2 p.47-58
Publication Date: Feb. 1992 Country of Publication: USA
CODEN: ECJSER ISSN: 1042-0967
U.S. Copyright Clearance Center Code: 1042-0967/92/0002-0047$7.50/0
Language: English Document Type: Journal Paper (JP)
Treatment: New Developments (N); Practical (P); Theoretical (T)
Abstract: A novel adder and multiplier using Hopfield-type neural networks, for which a technique is **introduced** to avoid **false operations**, is proposed. The simulation results for these operations are illustrated. The main feature of these circuits is high-speed operation which is achieved at almost constant computation time due to their parallel calculation ability. The authors describe in detail the technique to avoid false operations. It is important to determine the ratio of weight of the object function to constraint function. Computer simulations for the adder verify that the **correct operation** can be achieved by choosing the special ratio of the weight for these functions. The multiplier described is composed of the proposed adder and a neural network to perform the logical product. The simulation results for the multiplier show that the **correct operations** of a multiplication can be achieved with high-speed performance. (6 Refs)
Subfile: B C
Descriptors: adders; errors; multiplying circuits; neural nets
Identifiers: neural network digital multiplier; neural network digital adder; Hopfield-type neural networks; false operations; simulation results; high-speed operation; constant computation time; parallel calculation ability; object function; constraint function; logical product
Class Codes: B1265B (Logic circuits); B1295 (Neural nets); C5230 (Digital arithmetic methods); C5290 (Neural computing techniques)

18/5/8 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

03655107 INSPEC Abstract Number: B86026572
Title: Accelerated test method for false alarm characteristics of auto-alarm receivers
Author(s): Masuzawa, H.; Ichino, Y.; Chino, R.
Journal: Review of the Radio Research Laboratories vol.31, no.160 p.125-37
Publication Date: Sept. 1985 Country of Publication: Japan
CODEN: DKKIBA ISSN: 0033-801X
Language: Japanese Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: Describes a new accelerated test method of evaluating the false alarm characteristics of auto-alarm receivers aboard ships in a frequency band of 2182 kHz as well as test results. The qualification of the telephonic auto-alarm receivers is legally prescribed to take a type approval test by the domestic law domestically in conformity with the SOLAS (Safety of Life at Sea) Treaty. In this test, the evaluation of the false alarm characteristics is specially important. It requires, however, more than one year to confirm these characteristics because the actual interference conditions caused by signals and various noises are unpredictable and uncontrollable. The newly developed accelerated test method aims at increasing the **number** of occurrence of **erroneous operations** by simultaneously **adding** the auto-alarm signals and interference radio noises to the testing receivers. As the result of tests made by this method, the required **time** for confirming the characteristics of false alarms of an auto-alarm receiver is remarkably reduced to less than one day. (3 Refs)
Subfile: B
Descriptors: alarm systems; automatic testing; life testing
Identifiers: false alarm characteristics; auto-alarm receivers; accelerated test method; ships; frequency band; 2182 kHz; telephonic auto-alarm receivers; SOLAS; interference conditions; interference radio noises
Class Codes: B0160 (Plant engineering, maintenance and safety); B7210B (Automatic test and measurement systems)

18/5/9 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

02410171 INSPEC Abstract Number: B79043755
Title: Action of interference in control radio links
Author(s): Ganesan, S.
Author Affiliation: Systems Div., Nat. Aeronautical Lab., Bangalore, India
Journal: Electro-Technology vol.22, no.2 p.21-30
Publication Date: June 1978 Country of Publication: India
CODEN: ELTEAQ ISSN: 0013-4643
Language: English Document Type: Journal Paper (JP)
Treatment: Applications (A); Theoretical (T)
Abstract: The expressions for the calculation of average **number** of false **code** groups due to interference, the probability of suppression of one of the pulses of the code, and the average **number** of **false code** groups formed per **second** due to i false pulses **combining** with (n-i) pulses of any command code are given. The design of a **two** stage correlation **code** , which is secure against both random interference pulses and suppression of transmitted pulses, is discussed. Codes with repetition **interval** determined by pseudorandom generator and which are secure against synchronous or repeater jamming are explained. (7 Refs)

Subfile: B
Descriptors: interference suppression; radio links; radiofrequency interference
Identifiers: false code groups; command code; **two** stage correlation **code** ; random interference; repeater jamming; control radio links; radio interference suppression
Class Codes: B5230 (Electromagnetic compatibility and interference); B6250 (Radio links and equipment)

18/5/10 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

0000487412 INSPEC Abstract Number: 1958B03757
Title: A new voice-frequency receiver for long distance dialling
Author(s): Schmidt, W.
Journal: Nachrichtentechnik 7 11 p.495-501
Publication Date: Nov. 1957 Country of Publication: Germany
Language: German Document Type: Journal Paper (JP)
Abstract: Description of a voice-frequency receiver developed in East Germany and satisfying the latest C.C.I.F. recommendations. Main points of the technical specification are produced. The circuit diagram is shown of the receiver as used for single-frequency operation. The receiver, connected to the line via a differential transformer, contains a valve limiter, a bridge filter tuned to the signal frequency, and a thyratron valve with a relay in its anode. The thyratron is fired and switched off in rapid succession by an interrupter circuit, so as to check continuously the presence of the signal and to de-energize the relay at once when the signal ends. Other voice-frequencies can only cause the blocking-off of the thyratron, thus preventing **false operation** . By **adding** a **second** bridge filter and thyratron, the receiver can be used for **two** -frequency **operation** . Supervisory arrangements, necessary because of the thyratrons, are described. Operational results are given and compared with the C.C.I.F. recommendations.

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File 348:EUROPEAN PATENTS 1978-2006/ 200611
         (c) 2006 European Patent Office
File 349:PCT FULLTEXT 1979-2006/UB=20060316,UT=20060309
         (c) 2006 WIPO/Univentio

Set     Items   Description
S1       5548   (DUMMY OR FAKE OR FALSE OR GARBAGE OR NONSENSE OR JUNK OR -
            RUBBISH OR BOGUS OR PHONY OR MOCK OR MISLEADING OR ERRONEOUS -
            OR AMBIGUOUS OR USELESS)(2W)(INSTRUCTION? ? OR OPERATION? ? OR
             COMMAND? ? OR CODE? ? OR ACTION? ? OR TASK? ?)
S2        234   (DUMMY OR FAKE OR FALSE OR GARBAGE OR NONSENSE OR JUNK OR -
            RUBBISH OR BOGUS OR PHONY OR PHONEY OR MOCK OR MISLEADING OR -
            ERRONEOUS OR AMBIGUOUS OR USELESS)(2W)(JOB? ? OR TRANSACTION?
            ? OR CODEWORD? ?)
S3       2659   (PHONEY OR INVALID?)(2W)(INSTRUCTION? ? OR OPERATION? ? OR
            COMMAND? ? OR CODE? ? OR ACTION? ? OR TASK? ? OR JOB? ? OR TR-
            ANSACTION? ?)
S4       1681   S1:S3(10N)(INTRODUC? OR INPUT???? OR ADD??? OR INSERT??? OR
             ENTER??? OR GENERAT??? OR CREAT??? OR MIX??? OR INTERLEAV???
            OR COMBIN? OR MERG??? OR SLOT???? OR INCORPORAT? OR PRODUC????
             OR INTERSPERS? OR INTERMINGL???)
S5         77   S1:S3(10N)(INTEGRAT? OR MIX??? OR INTERMIX??? OR SPRINKL??-
            ?)
S6     141465   (SUCCEEDING OR SUCCESSIVE OR CONSECUTIV? OR ENSUING OR TWO
            OR SECOND???)(5W)(INSTRUCTION? ? OR OPERATION? ? OR COMMAND? ?
             OR CODE? ? OR ACTION? ? OR TASK? ?)
S7      54565   (THREE OR THIRD OR FOUR OR FOURTH OR FIVE OR FIFTH)(5W)(IN-
            STRUCTION? ? OR OPERATION? ? OR COMMAND? ? OR CODE? ? OR ACTI-
            ON? ? OR TASK? ?)
S8    1779486   TIME? ? OR TIMING OR INTERVAL? ? OR PERIOD? ? OR SECOND? ?
            OR MINUTE? ? OR HOUR? ?
S9        101   S1:S3(10N)(COMBIN??? OR COMBINATION? ?)
S10       196   (S4:S5 OR S9)(100N)S6:S7(100N)S8
S11    109694   S6:S7(50N)S8
S12       127   (S4:S5 OR S9)(100N)S11
S13        37   S12 AND AC=US AND AY=1970:1999
S14        74   S12 AND PY=1970:1999
S15    104267   (USEFUL OR FUNCTIONAL OR PROPER OR CORRECT OR NORMAL OR RE-
            GULAR OR RIGHT OR ACTIVE OR VALID OR LEGITIMATE)(2W)(INSTRUCT-
            ION? ? OR OPERATION? ? OR COMMAND? ? OR CODE? ? OR ACTION? ? -
            OR TASK? ? OR JOB? ? OR TRANSACTION? ?)
S16      5565   (SUCCEEDING OR SUCCESSIVE OR CONSECUTIV? OR ENSUING OR TWO
            OR SECOND??? OR SAME OR EQUAL OR IDENTICAL OR THREE OR THIRD -
            OR FOUR OR FOURTH OR FIVE OR FIFTH OR NUMBER OR AMOUNT)(5W)S15
S17        23   S4:S5(100N)S16(100N)S8
S18         9   S17 AND AC=US/PR AND AY=(1978:1999)/PR
S19         9   S17 AND AC=US AND AY=1978:1999
S20         9   S17 AND AC=US AND AY=(1978:1999)/PR
S21        12   S17 AND PY=1978:1999
S22        14   S18:S21
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22/3,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01267723
Media system and remote control for controlling the media system
Mediasystem und Fernsteuereinrichtung zur steuerung von das Mediasystem
Systeme de media et dispositif de telecommande pour commander le systeme de media
PATENT ASSIGNEE:
UNIVERSAL ELECTRONICS, INC., (1396114), 6101 Gateway Drive, Cypress, California 90630-4841, (US), (Applicant designated States: all)
INVENTOR:
Young, Jeffrey, 443 North Flower Street, Orange, California 92868, (US)
Muncy, David J., Haydnstraat 28, 7582 EW Losser, (NL)
LEGAL REPRESENTATIVE:
Kinsler, Maureen Catherine et al (87471), Kilburn & Strode, 20 Red Lion Street, London WC1R 4PJ, (GB)
PATENT (CC, No, Kind, Date): EP 1093103 A1 010418 (Basic)
APPLICATION (CC, No, Date): EP 309027 001013;
PRIORITY (CC, No, Date): US 418091 991014
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS (V7): G08C-019/28
ABSTRACT WORD COUNT: 179
NOTE:
Figure number on first page: 1

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200116	1314
SPEC A	(English)	200116	7098
Total word count - document A			8412
Total word count - document B			0
Total word count - documents A + B			8412

...SPECIFICATION lt;<Magic>> 4-1-2.
The units LED may be configured to blink two **times** after successful completion of the programming sequence. The unit may again be set to **time** out after 10 **seconds** of programming.
A Manufacturing Reset feature functions the same as the Operational Reset with the exception that...

...lt;Magic>> 4-1-1.
The unit's LED may be configured to blink two **times** followed by a short delay then blink two more **times** after successful completion of the programming sequence.
Set up using the Magic key is as follows. The...

...are assigned as follows:
After releasing the Magic key, the LED may be set to blink two **times** for verification. The LED shall blink once after each digit entry except for the last digit and shall blink **two times** to confirm that a **valid code** has been programmed. The unit shall turn off the LED, automatically exiting the programming mode and return...

...last program mode will be restored under two conditions: 1) when the six digit code is not **entered** within 10 **seconds** , and 2) when an **invalid code** is **entered** upon which the LED shall display a long blink. The programming mode shall be exited at any **time** by pressing any key other than the digit key.
To conserve battery power and avoid "mis-signaling...

22/3,K/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01030324
MOBILE ELECTRONIC COMMERCE SYSTEM
MOBILES ELEKTRONISCHES HANDELSSYSTEM
SYSTEME DE COMMERCE ELECTRONIQUE MOBILE
PATENT ASSIGNEE:
MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD, (216884), 1006, Oaza-Kadoma, Kadoma-shi, Osaka 571-0000, (JP), (Applicant designated States: all)
INVENTOR:
TAKAYAMA, Hisashi, 5-6-12-104, Matsubara, Setagaya-ku, Tokyo 156-0043, (JP)
LEGAL REPRESENTATIVE:
Grunecker, Kinkeldey, Stockmair & Schwanhausser Anwaltssozietat (100721), Maximilianstrasse 58, 80538 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 950968 A1 991020 (Basic)
WO 9909502 990225
APPLICATION (CC, No, Date): EP 98937807 980813; WO 98JP3608 980813
PRIORITY (CC, No, Date): JP 97230564 970813
DESIGNATED STATES: DE; FR; GB
RELATED DIVISIONAL NUMBER(S) - PN (AN):
(EP 2004015278)
INTERNATIONAL PATENT CLASS (V7): G06F-017/60
ABSTRACT WORD COUNT: 150
NOTE:
Figure number on first page: 1

LANGUAGE (Publication,Procedural,Application): English; English; Japanese
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9942	17239
SPEC A	(English)	9942	160346
Total word count - document A			177585
Total word count - document B			0
Total word count - documents A + B			177585

...SPECIFICATION ticket.
Since the matching of the generation order for the ticket examination response message and the remaining **amount** can be determined, a more precise examination of the validity of the ticket examination response message can be performed.
According to the invention cited in claim 132, at a **time** designated by the service providing means, the electronic ticket examination means generates an upload data message that includes data stored in the **second** storage means for the electronic ...transmits, to the electronic ticket examination means, an update data message that includes update data for the **second** storage means for the electronic ticket examination means; the electronic ticket examination means extracts the update data from the update data message that is received, and updates data stored in the **second** storage means.
Therefore, the ticket examination response can be automatically compiled, and its validity can be examined...

22/3,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00975324
Pipeline decoding system
Pipeline-System zur Dekodierung
Systeme pipeline de decodage

PATENT ASSIGNEE:
Discovision Associates, (260275), 2355 Main Street, Suite 200, Irvine, CA 92614, (US), (Proprietor designated states: all)
INVENTOR:
Wise, Adrian Philip, 10 Westbourne Cottages, Frenchay, Bristol BS16 1NA, (GB)
Sotheran, Martin William, The Ridings, Wick Lane, Stinchcombe, Dursley, Gloucestershire GL11 6BD, (GB)
Robbins, William Philip, 19 Springhill, Cam, Gloucestershire GL11 5PE, (GB)
Finch, Helen Rosemary, Tyley, Coombe, Wotton-Under-Edge, Gloucesterhire GL12 7ND, (GB)
Boyd, Kevin James, 21 Lancashire Road, Bristol BS7 9DL, (GB)
LEGAL REPRESENTATIVE:
Vuillermoz, Bruno et al (72791), Cabinet Laurent & Charras B.P. 32 20, rue Louis Chirpaz, 69131 Ecully Cedex, (FR)
PATENT (CC, No, Kind, Date): EP 884910 A1 981216 (Basic)
EP 884910 B1 010509
APPLICATION (CC, No, Date): EP 98202132 950228;
PRIORITY (CC, No, Date): GB 9405914 940324
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IE; IT; LI; NL
RELATED PARENT NUMBER(S) - PN (AN):
EP 674443 (EP 95301301)
INTERNATIONAL PATENT CLASS (V7): H04N-007/24; G06F-013/00; G06F-009/38
ABSTRACT WORD COUNT: 104
NOTE:
Figure number on first page: 76

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	199851	498
CLAIMS B	(English)	200119	330
CLAIMS B	(German)	200119	308
CLAIMS B	(French)	200119	382
SPEC A	(English)	199851	126705
SPEC B	(English)	200119	122739
Total word count - document A			127222
Total word count - document B			123759
Total word count - documents A + B			250981

...SPECIFICATION HIGH, meaning that the data on the transmission line into the pipeline is valid.

Also at this **time** , the ACCEPT signal into pipeline stage F is LOW, so that no data, whether valid or not, is transferred out of Stage F. Note that both valid and **invalid** data is transferred between pipeline stages. Invalid data, which is data not worth saving, may be written... may act upon them if required.

Figs. 9a and 9b taken together illustrate an example of a **timing** diagram for the data duplication circuit shown in Figs. 8a and 8b. As before, the **timing** diagram shows the relationship between the two-phase clock signals, the various internal and external control signals...

...from the input latches 34 is passed over line 32 to a token decode subsystem 33. A **second** output from the input latches 34 is passed as a first input over line 35 to a...

...36. A first output from the token decode subsystem 33 is passed over line 37 as a **second** input to the processing unit 36. A **second** output from the token decode 33 is passed over line 40 to an action identification unit 39, The **action** identification unit 39 also receives **input** from registers 43 and 44 over line 46. The registers 43 and 44 hold the state of...

...is passed to output latches 41. The output from the output latches 41 is

passed over a **second** bus 42.
Referring now to Figure 11, a Start Code Detector (SCD) 51 receives input over a...

...54 is logically passed over line 55 as a first input to a Huffman decoder 56. A **second** output from the Start **Code** Detector 51 is passed over line 57 as a first input to a DRAM interface 58. The...

22/3,K/4 (Item 4 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00625938
ANALOG-TO-DIGITAL CONVERTER AND METHOD OF FABRICATION
ANALOG/DIGITALWANLDER UND HERSTELLUNGSVERFAHREN
CONVERTISSEUR ANALOGIQUE/NUMERIQUE ET PROCEDE DE FABRICATION
PATENT ASSIGNEE:
HARRIS CORPORATION, (313793), 1025 West NASA Boulevard, Melbourne, FL 32901, (US), (applicant designated states: DE;FR;GB;IT)
INVENTOR:
BACRANIA, Kantilal, 1941 Brookside Street N.E., Palm Bay, FL 32907, (US)
CHI, Cong, In, 900 Pepper Tree Lane, Spt. 1111, Santa Clara, CA 95051, (US)
CHURCH, Michael, David, 355 Citrus Avenue, Sebastian, FL 32958, (US)
COTREAU, Gerald, M., 8615 Sheridan Road, Melbourne, FL 32904, (US)
DEJONG, Glenn, Alan, 10890 S. Tropical Trail, Merritt Island, FL 32952, (US)
FISHER, Gregory, James, 595 Seabreeze Drive, Indialantic, FL 32903, (US)
GASNER, John, Thomas, 509 Lanternback Island Drive, Satellite Beach, FL 32937, (US)
ITO, Akira, 2560 Lemmon Street N.E., Palm Bay, FL 32905, (US)
JOHNSTON, Jeffrey, Michael, 215 Rheine Road, N.W., Palm Bay, FL 32907, (US)
KING, Ken, Richard, 982 Emerald Road, S.E., Palm Bay, FL 32909, (US)
KUTCHMARICK, David, 3395 Church Road, Mountaintop, PA 18707, (US)
RHEE, Choong-Sun, 386 Lanack Road, S.E., Palm Bay, FL 32909, (US)
RIEMER, David, Wayne, 510 Banyan Way, Melbourne Beach, FL 32904, (US)
LEGAL REPRESENTATIVE:
Brandes, Jurgen, Dr. et al (2386), Wuesthoff & Wuesthoff Patent- und Rechtsanwalte Schweigerstrasse 2, 81541 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 610430 A1 940817 (Basic)
EP 610430 B1 990310
WO 9309599 930513
APPLICATION (CC, No, Date): EP 92924194 921029; WO 92US9366 921029
PRIORITY (CC, No, Date): US 785325 911030; US 785395 911030; US 785400 911030
DESIGNATED STATES: DE; FR; GB; IT
INTERNATIONAL PATENT CLASS (V7): H03K-005/15; H03K-005/13;
NOTE:
No A-document published by EPO
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	9910	1001
CLAIMS B	(German)	9910	974
CLAIMS B	(French)	9910	1174
SPEC B	(English)	9910	29364
Total word count - document A			0
Total word count - document B			32513
Total word count - documents A + B			32513

...SPECIFICATION of flash converter 306, and the headroom (see Figure 39) available in flash converter 306 on the **second** flash conversion permits the correction as follows. If flash converter 306 outputs a code that is

1...

...output an amplified quantization error that is 1.25 volts lower than it should be. Thus the **second** quantization by flash converter 306 is one lower in C6 than it should be, and this precisely...

...100. But presume flash converter 306 fails to be truly linear and outputs 1011 101 for this **input** . Then DAC 310 will reconstruct Vrq)) using the **erroneous code** 1011 101 and output 1.13281 volts as Vrq)). Now the quantization error Vin))-Vrq)) equals -0...

...625 volt. Now flash converter 306 quantizes -1.05 volts as -1.0547 volts which is -27 **times** 39.0625 mV and outputs 0100101 because 100101 is the two's complement of 011011 which is...

...the computations are as follows. Substractor 316 finds B12 B11 ... B6: This compares to B12 B11 ... B6 **equal** to 1011 010 for the **correct code** case. Next, error correction 318 adds C7 C6 to find D12 D11 .. D6: and filling in the...

22/3,K/5 (Item 5 from file: 348)

00592070

Recording and reproducing apparatus
Aufzeichnungs- und Wiedergabegerat
Appareil d'enregistrement et de reproduction

PATENT ASSIGNEE:
MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD., (216880), 1006, Ohaza Kadoma, Kadoma-shi, Osaka 571, (JP), (applicant designated states: DE;FR;GB)
INVENTOR:
Yamaguchi, Susumu, 10-21-103 Koshikiiwa-cho, Nishinomiya-shi, Hyogo-ken, (JP)
Matsumi, Chiyoko, 3-1-A3-202 Tsukumodai, Suita-shi, Osaka, (JP)
LEGAL REPRESENTATIVE:
Finsterwald, Manfred, Dipl.-Ing., Dipl.-Wirtsch.-Ing. et al (3691), Manitz, Finsterwald & Rotermund Patentanwalte Postfach 22 16 11, 80506 Munchen, (DE)

PATENT (CC, No, Kind, Date): EP 589459 A1 940330 (Basic)
EP 589459 B1 970806
APPLICATION (CC, No, Date): EP 93115375 930923;
PRIORITY (CC, No, Date): JP 92254317 920924
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS (V7): H04N-005/91; H04N-005/92;
ABSTRACT WORD COUNT: 230

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF2	1638
CLAIMS B	(English)	9708W1	928
CLAIMS B	(German)	9708W1	876
CLAIMS B	(French)	9708W1	1055
SPEC A	(English)	EPABF2	3719
SPEC B	(English)	9708W1	3752
Total word count - document A			5358
Total word count - document B			6611
Total word count - documents A + B			11969

...CLAIMS identification signal on the identification code input by the identification code input means and for outputting a **second** ID signal representing a result of the operation;
a comparator for comparing a value represented by the **second**

ID signal with a value represented by the reproduced first ID signal and for outputting a signal...

...recording medium is a magnetic tape or a nonvolatile memory provided in a cassette, wherein when an **erroneous** identification **code** is **input** to the first or **second** identification code **input** means, a **normal** reproducing **operation** is interrupted by ejecting the cassette, or turning off a power.

13. The recording and reproducing apparatus...

...recording medium is a magnetic tape or a nonvolatile memory provided in a cassette, wherein when an **erroneous** identification **code** is **input** to the identification code **input** means, a normal reproducing operation is interrupted by ejecting the cassette, or turning off a power. ...

...CLAIMS first operation circuit (103) outputs a signal representing the remainder as the first ID signal, and the **second** operation circuit (207) outputs a signal representing the remainder as the **second** ID signal.

5. The recording and reproducing apparatus according to claim 2 or 3, wherein the identification...

...medium is a magnetic tape (111) or a nonvolatile memory provided in a cassette, wherein when an **erroneous** identification **code** is **input** to the first or **second** identification code **input** means, a **normal** reproducing **operation** is interrupted by ejecting the cassette, or turning off a power.

9. The recording and reproducing apparatus **erroneous** identification **code** is **input** to the identification code **input** means, a normal reproducing operation is interrupted by ejecting the cassette, or turning off a power.

22/3,K/6 (Item 6 from file: 348)

00355124

Electronic controller switch.
Elektronischer Steuerungsschalter.
Commutateur de commande electronique.

PATENT ASSIGNEE:
SECURE-TIME, INC., (1170450), 2020 Avon Circle, Hayden Lake Idaho 83835, (US), (applicant designated states: AT;BE;CH;DE;ES;FR;GB;GR;IT;LI;LU;NL;SE)
INVENTOR:
Ratliff, James E., HC12 Box 461, Coeur D'Alnee Idaho 83814, (US)
Nicholson, Walter P., 1543 Hayden View Drive, Coeur D'Alnee Idaho 83814, (US)
LEGAL REPRESENTATIVE:
Patentanwalte Grunecker, Kinkeldey, Stockmair & Partner (100721), Maximilianstrasse 58, D-8000 Munchen 22, (DE)

PATENT (CC, No, Kind, Date): EP 371451 A2 900606 (Basic)
EP 371451 A3 910403
APPLICATION (CC, No, Date): EP 89121918 891128;
PRIORITY (CC, No, Date): US 276694 881128
DESIGNATED STATES: AT; BE; CH; DE; ES; FR; GB; GR; IT; LI; LU; NL; SE
INTERNATIONAL PATENT CLASS (V7): G07F-007/00; G07C-009/00;
ABSTRACT WORD COUNT: 231

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count
CLAIMS A (English) EPABF1 4291
SPEC A (English) EPABF1 7096

Total word count - document A 11387
Total word count - document B 0
Total word count - documents A + B 11387

...SPECIFICATION motels, hotels, or other similar environments, or for construction equipment which is often rented based on operation **time** . The microprocessor 106 is further coupled to a plurality of peripheral circuits 120, which are typically necessary...

...peripheral circuits 120 include a battery for storing electrical energy usable by the electronic controller switch during **periods** of power shortage or when the switch 100 is disconnected from the power source 104, such as...

...light-emitting diodes (LEDs) wherein each diode is indicative of the status of an operational parameter. The **three** LEDs indicate whether a **valid** input **code** has been supplied to the microprocessor by the user, whether an **invalid input code** has been supplied by the user, and whether power is being supplied to the device 102 by...

22/3,K/8 (Item 8 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00207293
Semiconductor switching device.
Halbleiterschalter.
Dispositif de commutation a semiconducteurs.
PATENT ASSIGNEE:
HITACHI, LTD., (204144), 6, Kanda Surugadai 4-chome, Chiyoda-ku, Tokyo 100, (JP), (applicant designated states: DE;GB;NL)
INVENTOR:
Ueno, Masahiro, Onuma Danchi 19-9, Higashionumacho-2-chome Hitachi-shi, (JP)
Iwamura, Masahiro, 10-9, Hanayamacho-1-chome, Hitachi-shi, (JP)
Masuda, Ikuro, 15-7, Moriyamacho-2-chome, Hitachi-shi, (JP)
Kurita, Kozaburo, 8-18, Kokubuncho-3-chome, Hitachi-shi, (JP)
LEGAL REPRESENTATIVE:
Patentanwalte Beetz sen. - Beetz jun. Timpe - Siegfried - Schmitt-Fumian (100711), Steinsdorfstrasse 10, W-8000 Munchen 22, (DE)
PATENT (CC, No, Kind, Date): EP 213608 A2 870311 (Basic)
EP 213608 A3 890802
EP 213608 B1 921028
APPLICATION (CC, No, Date): EP 86111893 860828;
PRIORITY (CC, No, Date): JP 85189643 850830
DESIGNATED STATES: DE; GB; NL
INTERNATIONAL PATENT CLASS (V7): H03K-017/687; H01L-027/06;
ABSTRACT WORD COUNT: 153

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	435
CLAIMS B	(German)	EPBBF1	414
CLAIMS B	(French)	EPBBF1	478
SPEC B	(English)	EPBBF1	7298

Total word count - document A 0
Total word count - document B 8625
Total word count - documents A + B 8625

...SPECIFICATION for a case where the Schottky diodes 120 to 126 are omitted from the PLA of Fig. **1** , to clarify the function of each Schottky diode. Similarly to the case where the Schottky diodes 121...

...the following reason. The second column line 172 kept at the low level is connected to the **second** row line 161 through the turned-on NMOS transistor 134, and thus the **second** row line 161 is put to the low level. Further, the **second** row line 161 is connected to the **second** column line 171 through the turned-on NMOS transistor 133, and thus the **second column** line **171** is put to the low level. As a result, the output signal E(sub 2) takes the low level. That is, when the Schottky diodes are omitted, an **erroneous** logical **operation** is performed. In other words, the Schottky diodes 121 to **126** prevent the back flow of current, to perform a correct logical operation.

As is evident from the above explanation, in the present embodiment, a plurality of **unidirectional** switching circuits each made up of one of the Schottky diodes 121 **to** 126 and a corresponding one of the NMOS transistors 131 to 136 are combined with the NMOS lines, the number of **second** row lines, the number of first column lines and the number of **second** column lines are all made equal to three. The present invention is not limited to such a case, but is applicable to a PLA having **a** desired number of row lines and column lines. Further, the PMOS transistors and the NMOS transistors may...

22/3,K/10 (Item 2 from file: 349)

00389799 **Image available**

REAL-TIME, ON-LINE, CALL VERIFICATION SYSTEM
SYSTEME DE VERIFICATION D'APPELS EN LIGNE ET EN TEMPS REEL

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HERON Andrew,

Patent and Priority Information (Country, Number, Date):
Patent: WO 9730542 A1 **19970821**
Application: WO 97US2312 19970220 (PCT/WO US9702312)
Priority Application: US 96603231 19960220
Designated States:
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CA AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Fulltext Word Count: 4214
Patent and Priority Information (Country, Number, Date):
Patent: ... **19970821**
Fulltext Availability:
Detailed Description
Publication Year: **1997**

Detailed Description
... or, if
desired, can recreate a speech compressed version of the original audio signal so the elapsed **time** needed to listen to the conversation is less than the length of the original conversation. At the same **time** , the processor 44 couples the updated customer record stored in memory 42 to the display terminal 30...

...at
the verification station is inconsistent with the voice recording of the transaction, the validation agent may **insert** a code marking the record **invalid** , which **code** is stored with the record in the sound and screen server and the host

computer in the **same** manner as a record **valid** **code** . In a preferred embodiment of the invention, the validation agent can correct the client record via keyed...

...screen server to down load records for a particular campaign to the verification stations in order of **time** sequence of record receipt as each station becomes available after completing a previous verification.

As will be...

22/3,K/11 (Item 3 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00294703 **Image available**
A METHOD AND A DEVICE FOR STORING INFORMATION, IN PARTICULAR PIN CODES
PROCEDE ET DISPOSITIF DE MEMORISATION D'INFORMATIONS, EN PARTICULIER DES CODES DE NUMERO D'IDENTIFICATION PERSONNEL
Patent Applicant/Assignee:
HERTZBERGER Robert Eric,
KRONER David Otto,
Inventor(s):
HERTZBERGER Robert Eric,
KRONER David Otto,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9512852 A1 **19950511**
Application: WO 94EP3593 19941031 (PCT/WO EP9403593)
Priority Application: NL 931880 19931102
Designated States:
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AM AT AU BB BG BR BY CA CH CN CZ DE DK ES FI GB GE HU JP KE KG KP KR KZ
LK LT LU LV MD MG MN MW NL NO NZ PL PT RO RU SD SE SI SK TJ TT UA US UZ
VN KE MW SD SZ AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE BF BJ CF
CG CI CM GA GN ML MR NE SN TD TG
Publication Language: English
Fulltext Word Count: 4000

Patent and Priority Information (Country, Number, Date):
Patent: ... **19950511**
Fulltext Availability:
Detailed Description
Publication Year: **1995**

Detailed Description
... method according to the invention, wherein the first code word must be input before at least one **second** code word stored in a second memory associated with the first memory can be read.

Preferably said...a further 5 embodiment, in that a second (pseudo) code word is decoded by means of the **input** first (**invalid**) **code** word when a dissimilarity is detected. Consequently, when an **invalid** first **code** word is **input** a similar second (pseudo) code The advantage of this embodiment of the method according to the invention is that, also when an **invalid** first **code** word is **input** , a second, albeit a pseudo-code word is generated as a result of the method being used...

...not, the person having possession of the device will not be able to ascertain if

indeed the **correct** **second** **code** word is being provided in a deterministic manner.

Yet another improvement of the protected storage of the...

...said second code word is retrievable from the memory in decoded form after the first (valid or **invalid**) 5 **code** word has been **input** , as is the other, previously **input** information.

Another embodiment of the method according to the invention provides for the input of text parts...

22/3,K/12 (Item 4 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00235339 **Image available**
ANALOG-TO-DIGITAL CONVERTER AND METHOD OF FABRICATION
CONVERTISSEUR ANALOGIQUE/NUMERIQUE ET PROCEDE DE FABRICATION
Patent Applicant/Assignee:
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Inventor(s):
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CHI Cong In,
CHURCH Michael David,
COTREAU Gerald M,
DEJONG Glenn Alan,
FISHER Gregory James,
GASNER John Thomas,
ITO Akira,
JOHNSTON Jeffrey Michael,
KING Ken Richard,
KUTCHMARICK David,
RHEE Choong-Sun,
RIEMER David Wayne,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9309599 A2 **19930513**
Application: WO 92US9366 19921029 (PCT/WO US9209366)
Priority Application: US 91325 19911030; US 91395 19911030; US 91400 19911030
Designated States:
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JP KR AT BE CH DE DK ES FR GB GR IE IT LU MC NL SE
Publication Language: English
Fulltext Word Count: 33453

Patent and Priority Information (Country, Number, Date):
Patent: ... **19930513**
Fulltext Availability:
Detailed Description
Publication Year: **1993**

Detailed Description
... of flash converter 306, and the headroom (see Figure 39) available in flash converter 306 on the **second** flash conversion permits the correction as follows. If flash converter 306 outputs a code that is 1...

...output an amplified quantization error that is 1.25 volts lower than it should be. Thus the **second** quantization by flash converter 306 is one lower in C6 than it should be, and this precisely...

...100. But presume flash converter 306 fails to be truly linear and

outputs 1011 101 for this **input** .

Then DAC 310 will reconstruct Vq using the **erroneous** **code** 101 1 101 and output 1. 13281 volts as Vq. Now the quantization error Vi.-Vq equals ...

...to +0.625 volt.

Now flash converter 306 quantizes 05 volts as 0547 volts which is -27 **times** 39.0625 mV and outputs 0100101 because 100101 is the two's complement of 011011 which is...316 finds B12 B11 ... B&
1011 101
+ 1111 110
@@Ioffl oil
This compares to B12 B11 ... B6 **equal** to 1011 010 for the **correct** **code** case. Next, error
correction 318 adds C7 C6 to find D12 Di I .. D&